TAFE NSW

Amplifier Configurations Part 1

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Workbook

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Amplifier Configurations - Part 1

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Contents

Introduction _____ I-3

Textbooks _____ I-4

Lesson organiser _____ I-6

Required reading _____ R-1

Section 1 The p-n junction and bipolar junction transistors _____ 1-1

Skill Practice 1 _____ 1-21

Review questions _____ 1-29

Section 2 Transistor biasing circuits _____ 2-1

Skill Practice 2 _____ 2-21

Review questions _____ 2-31

Section 3 BJT amplifier configurations _____ 3-1

Skill Practice 3 _____ 3-23

Review questions _____ 3-33

Section 4 BJT amplifier AC parameters _____ 4-1

Skill Practice 4 _____ 4-21

Review questions _____ 4-31

Section 5 Fault-finding BJT amplifier circuits and testing BJTs _____ 5-1

Skill Practice 5A _____ 5-21

Skill Practice 5B _____ 5-31

Review questions _____ 5-35

Section 6 Junction field effect transistors _____ 6-1

Skill Practice 6 _____ 6-21

Review questions _____ 6-31

Section 7 JFET amplifier configurations and AC parameters _____ 7-1

Skill Practice 7 _____ 7-19

Review questions _____ 7-29

Section 8 MOSFET amplifiers _____ 8-1

Skill Practice 8 _____ 8-23

Review questions _____ 8-31

Appendices

1: Other base bias and voltage divider bias circuits

2: Section summaries

Answers Section 1 _____ A-1

Section 2 _____ A-3

Section 3 _____ A-8

Section 4 _____ A-10

Section 5 _____ A-14

Section 6 _____ A-16

Section 7 _____ A-20

Section 8 _____ A-24

Introduction

This workbook is the first of two that have been written to help students satisfy the assessment requirements for the following Units:

- UEEEC0066 - Troubleshoot amplifiers in an electronic apparatus

More information about electrotechnology training packages and the above Units can be found at www.training.gov.au/home/tga. Type the course/unit number in the "Quick search" and press return.

Textbooks

The following textbooks can be used to supplement the notes in this workbook. Most (if not all) of these books are available from the library in Building D.

- Bell (1986). *Electronics devices and circuits* (3rd edition). Reston Publishing.
- Boylestad & Nashelsky (2002). *Electronic Devices and Circuit Theory* (8th edition). Prentice Hall.
- Donovan (2002). *Electronics Mathematics* (2nd edition). Prentice Hall.
- Edwards & Myer (1993). *Electronics; a basic course* (2nd edition). McGraw Hill.
- Floyd (2002). *Electronic Devices* (6th edition). Prentice Hall.
- Gates (2001). *Introduction to electronics* (4th edition). Thompson Printing.
- Granger (2000). *Amplifiers*. Educational Texts.
- Hazen (1991). *Exploring Electronic Devices*. Saunders Publishing.
- Ludeman (1990). *Electronic Devices and Circuits*. Saunders Publishing.
- Malvino (1998). *Electronic Principles* (6th edition). McGraw Hill.
- Paynter & Boydell (2002). *Electronics Technology Fundamentals*. Prentice Hall.

Lesson organiser

The following is a suggestion only. It may be changed to meet student needs and/or different modes of delivery.

Lesson	Section	Topics and activities
Before starting (ideally)	Required reading	■ Work health and safety ■ Using sustainable energy practices ■ Communication and documentation ■ Test and measurement devices and their safe use
1	1	■ The p-n junction ■ BJT biasing requirements and transfer characteristics ■ Practise measuring DC currents in BJT circuits using a DMM
2	2	■ BJT biasing methods including: base bias and voltage divider bias ■ Practise measuring DC voltages in BJT amplifiers using a DMM
3	3	■ BJT amplifier configurations ■ Practise measuring AC voltages in BJT amplifiers using an oscilloscope
4	4	■ BJT amplifier parameters including: voltage gain, input resistance and output resistance ■ Practise measuring AC voltages in BJT amplifiers using an oscilloscope to determine input-output phase relationship, voltage gain and frequency response
5	5	■ Fault-finding BJT amplifier circuits ■ Testing BJTs ■ Practise trouble-shooting BJT amplifiers using a DMM and an oscilloscope ■ Testing transistors using the diode test mode of a DMM
6	6	■ JFET biasing requirements and transfer characteristics ■ JFET biasing methods including: self bias and voltage divider bias ■ Practise measuring DC voltages and currents in JFET amplifiers using a DMM
7	7	■ JFET amplifier configurations and parameters including: voltage gain, input resistance and output resistance ■ Practise measuring AC voltages in FET amplifiers using an oscilloscope to determine input-output phase relationship, voltage gain and frequency response
8	8	■ MOSFET biasing requirements and transfer characteristics ■ MOSFET biasing methods including: self bias and voltage divider bias ■ MOSFET amplifier configurations and parameters including: voltage gain, input resistance and output resistance ■ Practise measuring DC and AC voltages in MOSFET amplifiers using a DMM and an oscilloscope
9	**You will most likely have to complete the knowledge and performance assessments in this lesson. However, please refer to the Unit Assessment Guidelines (UAG) for the exact dates of all tests.**	

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Student notes

Required reading

Purpose

These notes are provided to support your revision on aspects of this Unit that have been taught before in other Units (typically more than once) and will not be taught again but may be assessed.

This issue is explained in more detail on the following pages.

Introduction

As you probably know, *units of competence* that make up qualifications in the Electrotechnology Training Package (like CIII Electronics and Communications) prescribe what must be taught and assessed.

This is done using *elements of competence* together with *performance criteria* for each element. More detail on these is provided in the *assessment requirements* for the unit using two lists: one is the list of *performance evidence*; and the other is the list of *knowledge evidence*.

There are some performance criteria (together with performance evidence and/or knowledge evidence in the assessment requirements) that appear in many units and these include items on the following topics:

- work health and safety (WHS)
- using sustainable energy practices
- the appropriate use and completion of documentation
- appropriate communication with supervisors, customers and other stakeholders.

It makes sense that these performance criteria are common to multiple units because, taking WHS as an example, it's not reasonable to claim competence when the work was completed successfully but in an unsafe way.

As well as the topics listed above, there are performance criteria and/or assessment requirements related to electrical/electronic theory and practice that appear in two or more units. This occurs when the people who have developed the training package (not TAFE NSW) have decided that it's appropriate that they should do so. An example of this for UEEEC0066 is the requirement for you to demonstrate your knowledge of how to connect a digital multimeter to a circuit to measure potential difference which you have previously learnt about when undertaking CD0043 (formerly UEENEEE104A).

Importantly, where all these topics have been comprehensively taught before, it is usually unnecessary to teach them a second or third time. That said, we are still expected to ask you to provide knowledge evidence and/or performance evidence possibly by answering questions on these topics in the theory test and/or demonstrating your skills on these topics during the practical tests.

For this reason, the following information and/or notes are provided for you to read and use to ensure that you can satisfy the assessment requirements for this unit.

Work health and safety (WHS)

When you undertake the in-class simulated workplace tasks and/or the practical test for this unit (EC0066), you're expected to demonstrate your knowledge of, and demonstrate your ability to carry out, the following performance criteria related to WHS and their associated knowledge evidence and performance evidence:

1.1 - WHS requirements and workplace procedures for relevant work area are identified, obtained and applied (UEECD0007 references: 1.2, 1.3 & 1.4)

1.2 - WHS risk control measures are applied in accordance with workplace procedures prior to commencing work (UEECD0007 references: 1.2, 1.3 & 1.4)

2.1 - Workplace risk control measures and procedures are applied (UEECD0007 references: 1.4, 1.6, 2.1 and 2.4)

2.2 - The need to test or measure live work is determined, as required, in accordance with WHS requirements and workplace procedures (UEECD0007 references: 1.2, 1.3 & 1.4)

3.1 - WHS risk control measures and procedures are applied (UEECD0007 references: 3.1 to 3.4)

3.2 - Worksite is cleaned and made safe in accordance with workplace procedures (UEECD0007 references: 2.6)

Source: https://training.gov.au/Training/Details/UEEEC0066

As you may already be aware:

- WHS is taught and assessed in a dedicated unit, CD0007 (formerly E101A) and you should have a pass for this unit
- The performance criteria listed above are underpinned by, and/or are identical in substance to, the performance criteria from CD0007 (and E101A) indicated in the brackets above

Importantly, the knowledge and skills needed to perform these performance criteria are identical to those needed to repair amplifier circuits. This means that you already have the ability to demonstrate your knowledge of, and demonstrate your ability to carry out, these performance criteria in the context of this unit.

However, if your unsure and would like to read more information about these performance criteria, please refer to your learner resources for CD0007/E101A that specifically address them.

Note: If you have not successfully completed CD0007 or E101A, please bring this to the urgent attention of the teacher before undertaking any of the simulated workplace tasks.

Using sustainable energy practices

When you undertake the in-class simulated workplace tasks and/or the practical test for this unit (EC0066), you're expected to demonstrate your knowledge of, and demonstrate your ability to carry out, the following performance criterion:

2.6 - Fault-finding is conducted efficiently minimising waste of materials, damage to apparatus, the surrounding environment or services applying sustainable energy practices.

This includes knowing about sustainable energy principles and using sustainable energy practices.

Sustainability is a much used word now that describes growing global response to the short and long term negative effects on the planet of certain human activities, particularly in relation to climate change and pollution. It's accepted that, without drastic action, both problems will likely make living on this planet more difficult (due to extreme weather and toxic environments) that, in turn, risk causing drought, famine, war and the failure of democratic governments and even whole nation states.

R J Fuller (Deakin University, 2005) describes four principles that underpin sustainability:

- Futurity - The concern for future generations
- Environment - The concern to protect the integrity of eco-systems
- Equity - The concern for the poor and disadvantaged
- Participation - The notion that individuals can participate in decisions affecting them

An essential element of the global response to climate change is the switch to sustainable energy. Energy is said to be sustainable if it "meets the needs of the present without compromising the ability of future generations to meet their own needs." Underpinning this are the sustainable energy principles which include (but are not limited to):

- Reducing our use of non-renewable energy sources (like the fossils fuels which includes coal, gas and oil)
- Increasing our use of renewable sustainable energy sources (like solar just to name one of many).

Fuller's fourth principle is important because it means that individuals, including you, can contribute directly and indirectly to sustainable energy principles by using sustainable energy practices where possible. Direct action that can be taken includes (but is not limited to):

- Switching off equipment not in use
- Turning off lights when leaving a room with nobody in it
- Opening windows to cool rooms instead of turning on room air-conditioning
- Using natural lighting
- Minimising waste
- Recycling waste
- Using public transport to and from work
- Drinking tap water

Indirect action that can be taken, includes (but is not limited to) encouraging your employer to:

- Using more energy efficient lighting
- Using more energy efficient equipment
- Reducing (in winter) and increasing (in summer) the temperature setting of air conditioning so that to uses less energy
- Switching to using sustainably sourced and/or sustainably manufactured materials
- Switching to an SEU energy provider

With all that said, every workplace is different so what works with one may not work with another.

Communication and documentation

When you undertake the in-class simulated workplace tasks and/or the practical test for this unit (EC0066), you're expected to demonstrate your knowledge of, and demonstrate your ability to carry out, the following performance criteria related to workplace communication and documentation and their associated knowledge evidence and performance evidence:

1.3 - Nature of amplifier fault is obtained from documentation or from relevant person/s to determine scope of work

1.4 - Instructions for coordinating work with others are obtained from relevant person/s and applied

1.5 - Materials required for work are determined in accordance with workplace procedures

1.6 - Tools, equipment and testing devices required for work are obtained and checked for correct operation and safety

3.3 - Justification for troubleshooting solutions is provided in the required format

3.4 - Work completion is documented in accordance with workplace procedures and relevant person/s notified

The specific knowledge required to satisfy these performance criteria is specific to each workplace setting. However, the skills are generic and so are transferable between workplace settings including simulated workplace settings at TAFE NSW. This means that, when you undertake the in-class simulated workplace tasks and the practical test, you are expected to demonstrate your skills in this regard.

Importantly, while undertaking the in-class simulated workplace tasks and/or the practical tests for this unit at TAFE NSW, the following applies to key terms in the performance criteria above:

- "Relevant person/s" refers to the class teacher
- "Others" refers to the class teacher and other students in the class
- "Materials" refers to components and training aids needed to carry out the simulated workplace tasks as described in the skill practise exercises' equipment list
- "Workplace procedures" refer to the written and verbal procedures and instructions provided by the teacher for the safe and proper conduct of skill practise exercises
- "Tools, equipment and testing devices" refers to tools and test equipment needed to carry out the simulated workplace tasks as described in the skill practise exercises' equipment list and/or mounted on the workbenches

- "Work completion is documented..." refers to the requirement for students to record their measurements, other results, and answers to questions on the skill practice exercises and/or any handouts that must be submitted to the teacher.

The following is the procedural requirement for undertaking the simulated workplace tasks that form the basis of skill practise exercises.

- Students must have permission from the teacher to start every skill practice exercise.
- Students must work individually on every skill practise exercise, or in pairs with the permission of the teacher (but never more than two per group).
- Students must perform a WHS risk assessment at the start of every skill practice exercise to ensure the safety of themselves and others.
- Students are to bring to the attention of the teacher any hazards that they identify for which there are they cannot implement appropriate control measures.
- Students are to collect equipment from the trolley in a safe and orderly manner having respect for the reasonable needs of other students.
- Students are to follow the written instructions in every skill practice exercises in correct order and in total including any qualifying notes.
- Students are expected to record their measurements, other results and answers to questions for every skill practice exercise and/or any handouts that must be submitted to the teacher.
- Students are expected to call the teacher to check their work when instructions direct them to do so.
- Students are expected to retake any measurements and reattempt and/or correct any of their answers to questions when reasonably directed to do so by the teacher.
- Students are not to return their equipment to the trolley or leave **until** they have completed the skill practice exercise and their work has been checked by the teacher.
- Students are expected to submit their work to the teacher by the due date when required to do so.
- At the completion of every skill practice exercise, students are expected to return all equipment to the trolley tidily (unless directed otherwise by the teacher) and ensure that the workspace is left cleaned and safe.
- Students are to bring to the attention of the teacher any faulty test equipment, tools and components.

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Test and measurement devices and their safe use

When you undertake the in-class simulated workplace tasks and/or the practical test for this unit (EC0066), you're expected to demonstrate your knowledge of:

- Electronic testing and measuring devices and techniques including:
  - test/measuring devices and their application including:
    - multimeters
    - function generators
    - oscilloscopes
  - connection of test/measruing devices into a circuit including:
    - ensuring circuits are isolated
    - testing or measuring on live and operating system safely

You first learnt about multimeters and practised using them on live circuits when undertaking unit CD0043. And you have learnt about, or are currently learning about, the correct use of function generators and oscilloscopes in EC0074.

Importantly, you're expected to know the general principles of using multimeters, function generators and oscilloscopes the safety precautions around working on live circuits. However, if your unsure that you are able to demonstrate your knowledge of these tasks or your ability to carry them out, the following notes have been provided here for your convenience for you to read.

Safety considerations when connecting test and measurement devices to circuits
When using a multimeter or oscilloscope to test and measure electronics equipment, there are two important safety measures that can minimise the risk of your being fatally electrocuted.

The first relates to the fact that technicians usually must necessarily test mains-operated electronics equipment (like a hi-fi or PVR) that is plugged-in, turned on and operating. To minimise the risk of electrocution, you must ensure that the equipment that you're testing or repairing is plugged into a power point that is protected at the switchboard by a residual current device (RCD). You can check whether the building's powerpoints are RCD protected by looking inside the switchboard. Figure 1 below shows an example of what to look for.

Figure 1

Up close, RCDs look like the example in Figure 2 below and there should be at least one row of these devices in the switchboard mounted side-by-side. RCDs are easily recognised by the fact that they're switched devices and often they have an in-built test feature too.

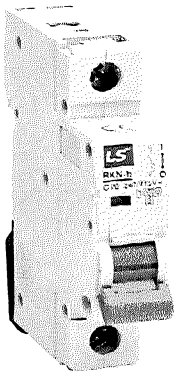

Figure 2

RCDs have been designed expressly for the purpose of preventing people and animals from a sustained direct connection to mains which can be fatal.

If the switchboard is older it may use semi-enclosed cartridge fuses instead of RCDs and an example is shown in Figure 3 below. Importantly, being fuses, these devices are designed to protect equipment and prevent fires but they **do not** prevent people/animals from potentially fatal electrocution. You should avoid powering the equipment that you're testing/reparing from power points that are only protected at the switchboard by these fuses.

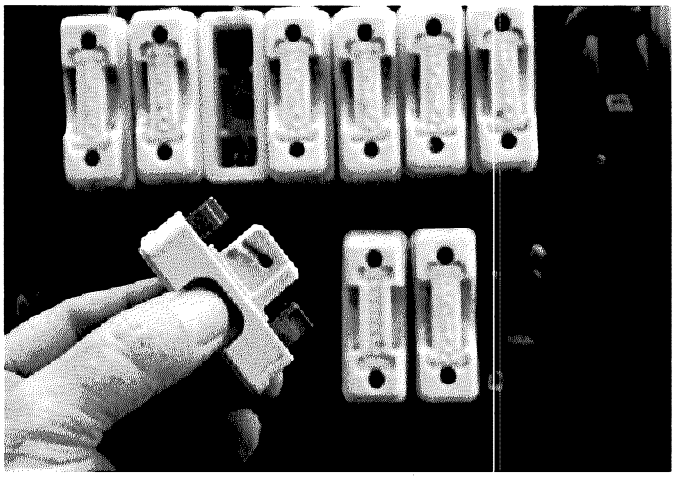

Figure 3

If you can't access the switchboard to see what's inside, or you know for certain that the power point is not RCD protected, then plug the equipment that you're testing into the powerpoint of a powerboard that is RCD protected instead. An example is shown in Figure 4 below - Notice the RCD at the left end (which includes a button for the test feature).

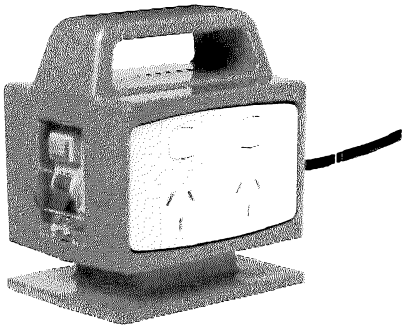

Figure 4

Take care when purchasing protected powerboards because there are many that offer "surge" and/or "overload" protection. While these features are useful, they don't provide protection from electrocution. Powerboards that are RCD protected will state this clearly and are usually a fair bit more expensive than simple surge and overload protected powerboards.

The second safety measure you must employ when connecting multimeters to live equipment, involves never doing so with your fingers touching any of the probe's metal parts. Figure 5 below shows the correct way to hold the probes. Notice that the person holds the probes behind the their slip barriers.

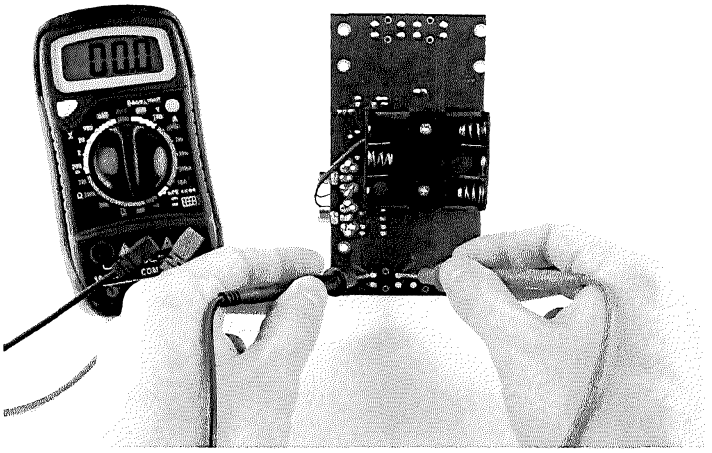

Figure 5

Similarly, when connecting oscilloscope probes to live equipment, ensure that your fingers don't make any contact with the circuit board or the probe's metal parts at the tip. Figure 6 below shows the correct way to hold oscilloscope probes. Notice that the person holds the probe behind the slip barrier if, they've rested their hand on the workbench not the circuit board.

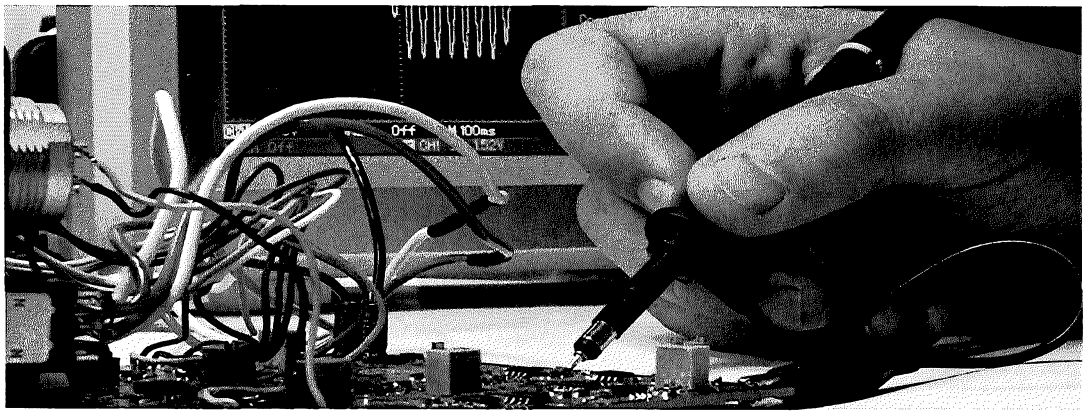

Figure 6

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Student notes

Section 1 Bipolar junction transistors

Purpose To develop your understanding of the basic operation of the bipolar junction transistor.

Objectives At the end of this section you should be able to:

- Draw and identify the schematic symbols for NPN and PNP bipolar junction transistors (BJTs)
- Name the three terminals of a BJT
- State the bias conditions needed for the junctions of an NPN and PNP BJT for them to operate in amplifier circuits
- State the DC terminal requirements needed to obtain the bias conditions for the junctions of an NPN and PNP BJT
- Show the direction of conventional current flow at each terminal of an NPN and PNP BJT
- Calculate either the base, emitter or collector currents of a BJT given values for two of the currents
- Explain the operating principle of a BJT
- Define the terms *cut-off*, *linear operation* and *saturation* as applied to BJT operation
- Identify a BJT's cut-off, linear region and saturation region in a graph of base current versus collector current
- Explain why a BJT is a current controlled device
- Explain why a BJT is a current amplifying device
- Define the term *beta* as used with BJTs
- Calculate either the beta, base current or collector current of a BJT given values for two of the quantities
- Verify the relationship between the base and collector current of a forward-biased BJT

Introduction

The invention of the transistor is often quoted as being the most important invention of the 20th century. Prior to transistors, amplification and switching in electronics systems were handled by devices called *valves* which are vacuum-sealed glass tubes through which electrons flow from one end to the other can and can be controlled by the application of a voltage on a third terminal.

Valves are physically large and take time to warm up so the transistor's advantages are obvious. Valves are also very inefficient and so transistors are a substantial improvement in this regard also. However, the transistor's claim to importance is probably due to the fact that it can be made so small that over ten million of them can be laid down on a 1mm^2 semiconductor wafer. This type of density allows the implementation of circuits with mind-boggling complexity in ICs only the size of a fingernail. For more on this, visit: https://en.wikipedia.org/wiki/Transistor_count.

As you're working in electronics and/or have an interest in it, you probably already know a little about transistors. This subject formally introduces transistors to you for the first time in the course. It covers the construction and operation of the two main groups of transistor and how they are operated in circuits.

Transistor types

As just mentioned, there are two main groups of transistor with variations of each. Figure 1 below shows the transistor's family tree.

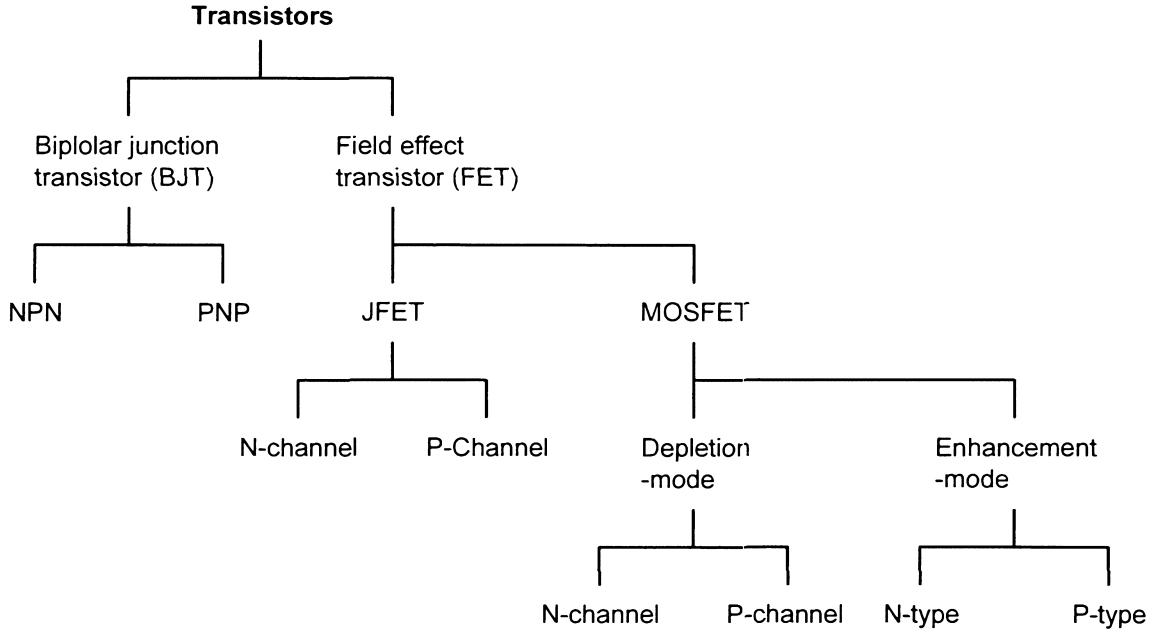

Figure 1 *The relationships between the different types of transistors*

A little history

Depending on what book or website you read, transistors were invented in 1947 or 1948 by Bell Telephone Laboratories physicists John Bardeen, Walter Brattain and William Shockley. Apparent confusion over the date exists because the very first operational transistor was achieved in December 1947 but not publicly announced until June 1948. Moreover, today's BJTs are based on a variation of this first transistor that was developed several months later so both dates are valid.

Regardless of which year the transistor was invented, it was an incremental development that followed over a hundred years of hypothesis and research by people of many nationalities. The existence of silicon for example was first theorised about in the late 1700s by a French chemist and was discovered in 1817 by a Swiss chemist (silicon doesn't exist in a "pure" form like gold does for example). The chemical properties and atomic structure of semiconductors were investigated throughout the 1800s and the practical applications of semiconductors to electronics were investigated in the 1900s between World Wars I & II by both U.S. and European physicists. Germans played a significant part here. Mott and Schottky proved the rectifier effect (using a normal metal and a semiconductor) and Pohl developed a semiconductor device with some of the elements of a transistor.

Research into radar systems during World War II lead to significant leaps in semiconductor technology and a leader in this area was the Bell Telephone Company which ultimately realised both types of transistor.

Interestingly, the bipolar junction transistor (BJT) was realised first, apparently by accident. At the time, Shockley's team was attempting to develop a *solid-state* analog of the valve which was invented several months later and became the field effect transistor (FET). The first licence to manufacture transistors was issued in 1951 and the semiconductor industry as we know it today was born.

Sources:

A book called *The electronic epoch* written by Elizabeth Antebi and published by Van Nostrand Reinhold Company (dated 1982).

And the following websites (which are no-longer available but other sites with the same information can be found using search terms borrowed from these URLs):

http://ourworld.compuserve.com/homepages/Andrew_Wylie/history.htm

http://encyclobeamia.solarbotics.net/articles/transistor.html

http://people.deas.harvard.edu/~jones/es154/lectures/lecture_4/lecture_4.html

http://nobelprize.org/physics/educational/transistor/history/

http://www.rohm.com/en/transistor/what1.html

The P-N junction

Key to the operation of all transistors is the P-N junction. Much has been written on this subject and there are excellent resources in several textbooks (especially by Floyd). As such, no notes are included here. Your teacher will explain P-N junction action at a level suitable to the class.

The bipolar junction transistor (BJT)

Bipolar junction transistors are three-terminal devices made from semiconductor materials such as *germanium* and *silicon*. Germanium was originally widely used for early transistors, however, it breaks down at lower temperatures than silicon and so silicon transistors are much more prevalent today.

The term *bipolar* is used because BJTs are made using both P-type and N-type semiconductors. Their construction is essentially a sandwich of one type of semiconductor between two layers of the other type. This means that it's possible to make two kinds of BJT: **NPN** and **PNP**.

NPN and PNP BJTs

The schematic symbol, physical construction and *two-diode representative model* for an NPN and a PNP transistor are shown in Figures 2 and 3.

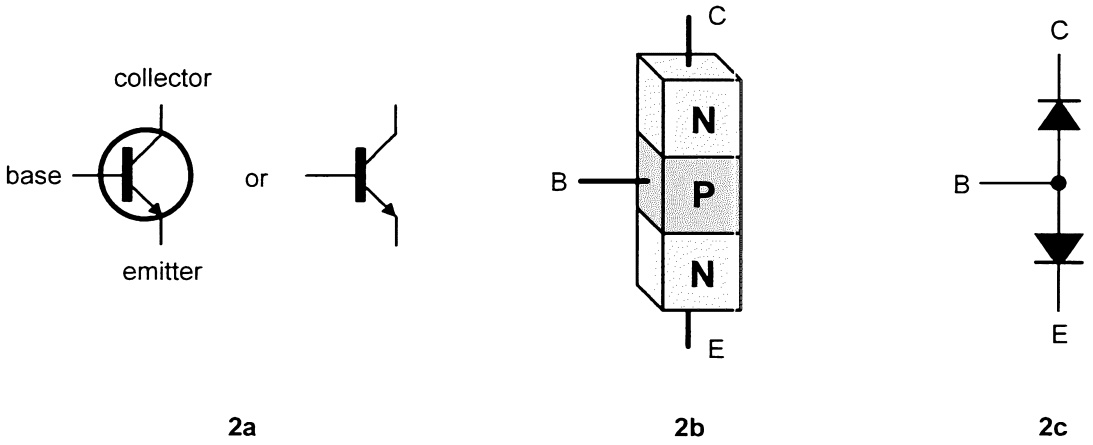

Figure 2 *(a) The schematic symbol, (b) the physical construction and (c) the two-diode representative model for an NPN transistor*

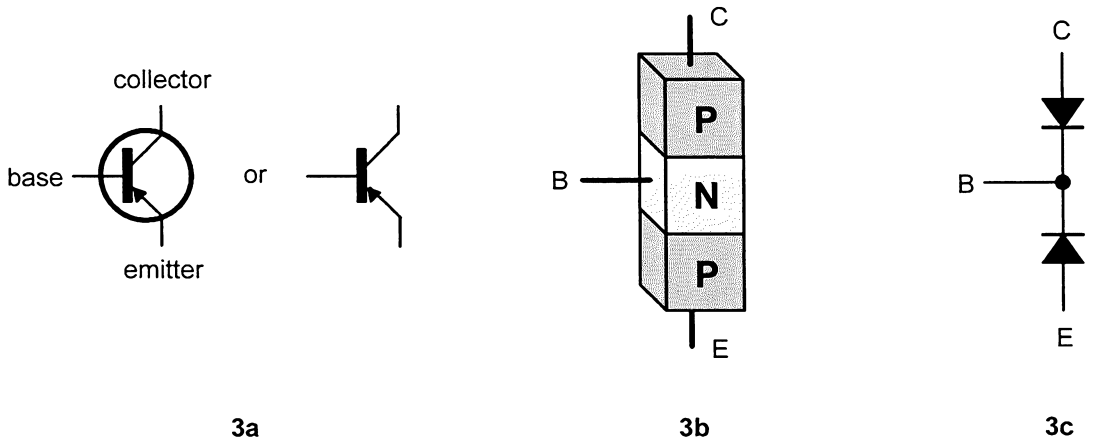

Figure 3 *(a) The schematic symbol, (b) the physical construction and (c) the two-diode representative model for a PNP transistor*

Figures 2a and 3a show the schematic symbol for an NPN and PNP transistor respectively. There are three things that you should notice about the schematic symbols:

- The base is the middle leg
- The emitter leg has the arrow in it
- The arrow points *out* for an NPN and *in* for a PNP

Figures 2b and 3b show the approximate physical construction of both transistors. As you can see, the NPN transistor is a sandwich of P-type semiconductor material between two layers of N-type material and the PNP transistor is a sandwich of N-type semiconductor material between two layers of P-type material.

Figures 2c and 3c show the two-diode representative model for each transistor. This model is used to help us understand how transistor biasing works and to help us test BJTs to determine whether they're functional. As you can see, the combination of n-p-n and p-n-p materials is the same as two diodes connected in series but pointing in opposite directions. However, this model is only a representation. Two diodes connected in series and back-to-back **wont** work as a transistor.

BJT operation

Put simply, the BJT is a current amplifier. So, to learn about its operation, we must learn about what currents flow through a BJT and their relationship to each other. However, to explain this, we must first discuss the BJT's operating (*biasing*) voltage requirements.

Biasing voltage requirements for BJTs

Figure 4 below shows the relative voltages needed on the terminals of an NPN BJT to bias it so that it will work in the amplifier circuits you will be learning about. Importantly, the circuit in Figure 4 is only a guide and is not a real circuit because it doesn't have any of the resistors necessary in a real circuit.

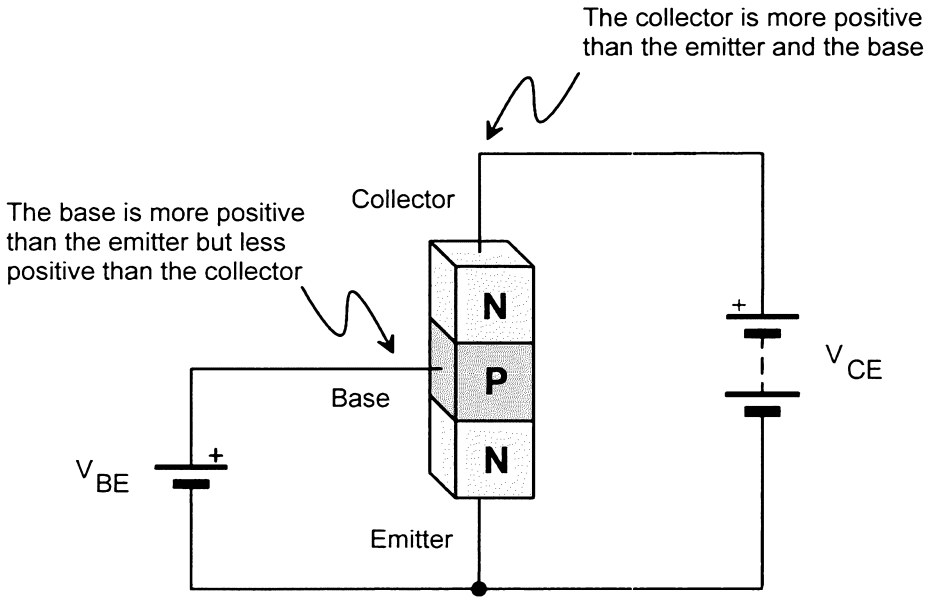

Figure 4 *The relative voltages needed on the terminals of an NPN BJT for it to work in amplifier circuits*

The diagram shows that an NPN BJT requires a DC voltage between the collector and the emitter (V_{CE}) that makes the collector more positive than the emitter. It also needs a DC voltage across the base-emitter junction (V_{BE}) that makes the base more positive than the emitter. However, the voltage on the BJT's base must be smaller (or less positive) than the voltage on its collector.

The BJT in the basic circuit in Figure 4 can be replaced by its two-diode representative model as shown in Figure 5 below. When it is, we can see that these relative voltages on the BJT's terminals set-up a collector-base p-n junction that is always reverse biased and a base-emitter p-n junction that may become forward biased provided V_{BE} is approximately 0.6V (the exact voltage varies from BJT to BJT but it will fall somewhere between about 0.5V and 0.7V).

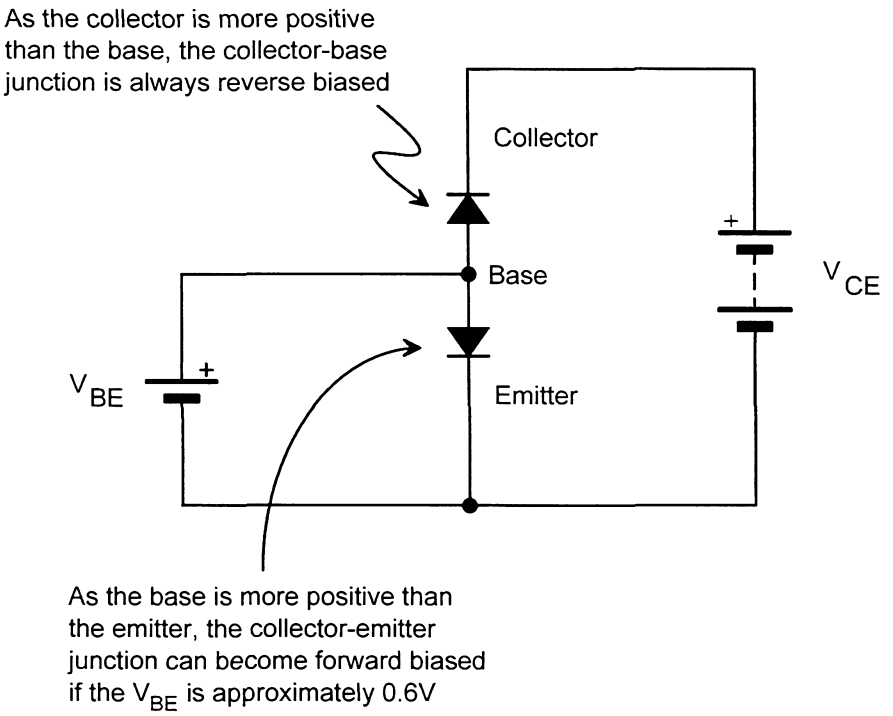
As the collector is more positive than the base, the collector-base junction is always reverse biased
Collector
Base
Emitter
+
V_{CE}
+
V_{BE}
As the base is more positive than the emitter, the collector-emitter junction can become forward biased if the V_{BE} is approximately 0.6V

Figure 5 *The simple biasing circuit in Figure 4 redrawn using the two-diode representative model*

Figure 6 below shows the relative voltages on the terminals of an PNP BJT to bias it so that it will work in the amplifier circuits you'll be learning about.

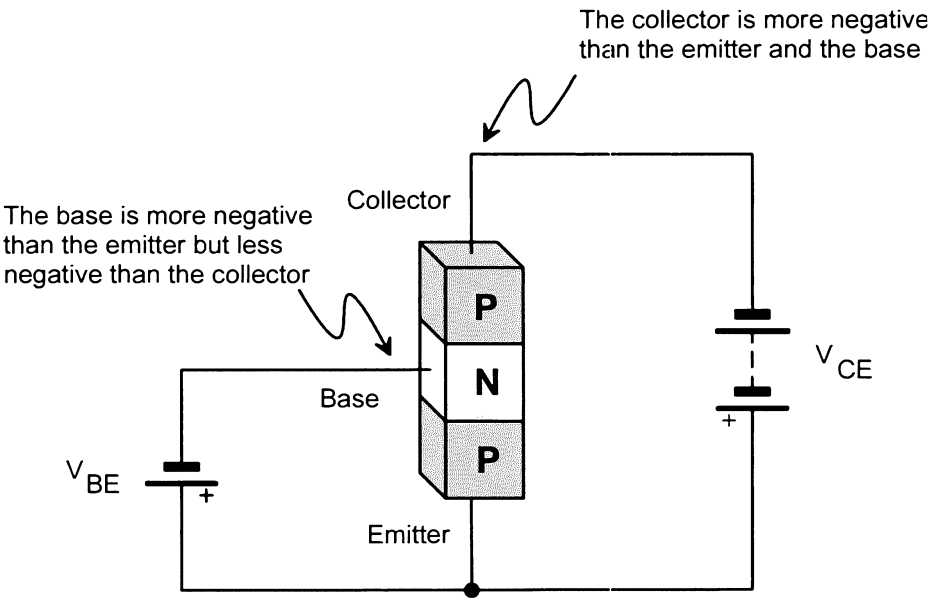

Figure 6 *The relative voltages needed on the terminals of a PNP BJT for it to work in amplifier circuits*

The diagram shows that a PNP transistor needs a DC voltage between the collector and the emitter (V_{CE}) that makes the collector more negative than the emitter. It also needs a DC voltage across the base-emitter junction (V_{BE}) that also makes the base more negative than the emitter. However, the voltage on the BJT's base must be smaller (or more positive) than the voltage on its collector.

Again, the BJT in the basic circuit in Figure 6 can be replaced by its two-diode representative model as shown in Figure 7 (on the next page). When it is, we can see that these relative voltages on the BJT's terminals set-up a collector-base p-n junction that is always reverse biased and a base-emitter p-n junction that may become forward biased provided V_{BE} is approximately -0.6V (the exact voltage varies from BJT to BJT but it will fall somewhere between about -0.5V and -0.7V).

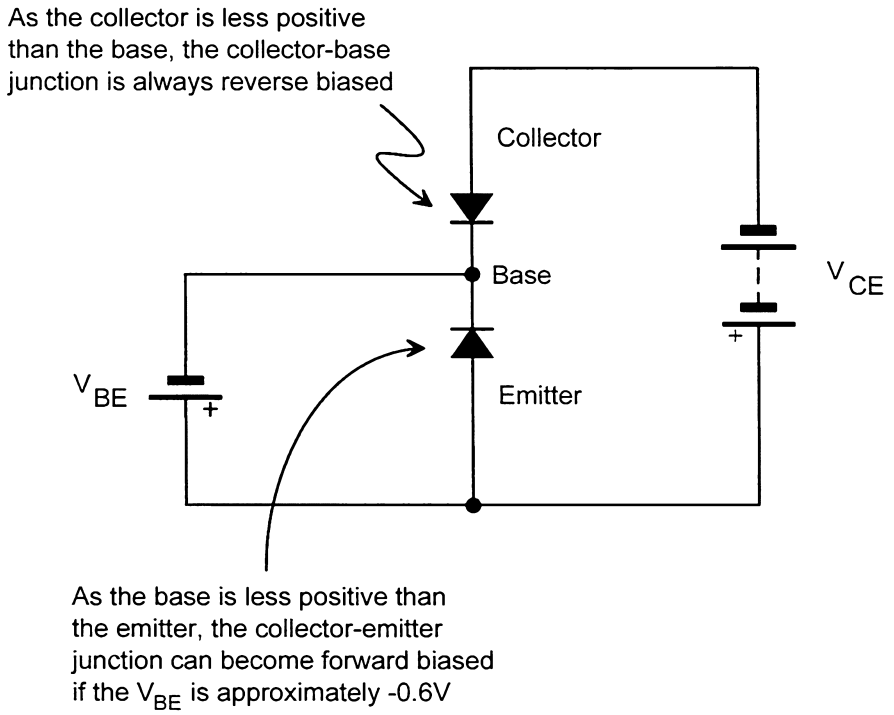
As the collector is less positive than the base, the collector-base junction is always reverse biased
Collector
Base
Emitter
V CE
V BE
As the base is less positive than the emitter, the collector-emitter junction can become forward biased if the V BE is approximately -0.6V

Figure 7 *The simple biasing circuit in Figure 6 redrawn using the two-diode representative model*

The same relative DC voltages on the terminals of the PNP BJT above can be achieved by reversing the polarity of V_{BE} and V_{CE} and swapping the collector and emitter terminals. This is shown in Figure 8 below.

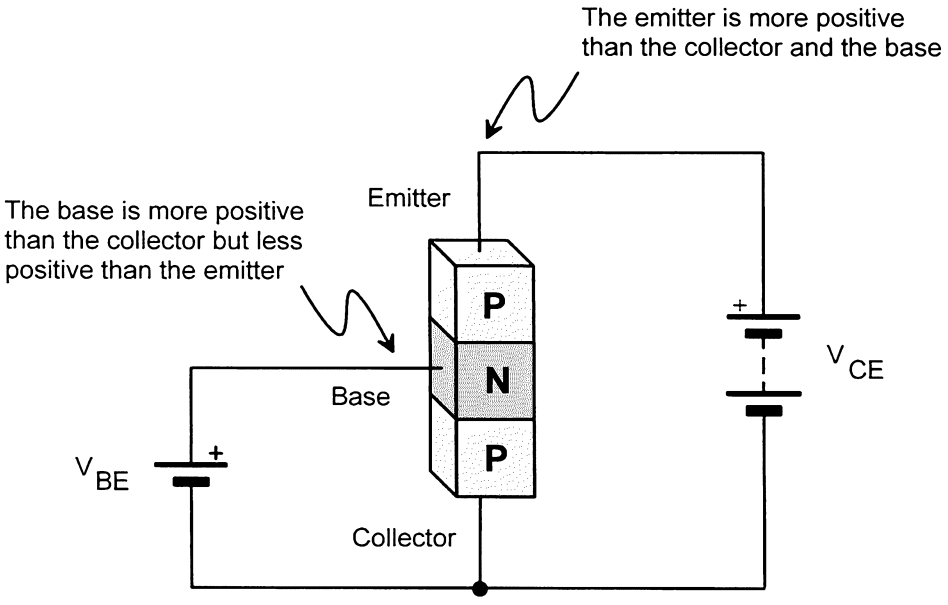

Figure 8 *The relative voltages needed on the terminals of a PNP BJT for it to work with a positive V_{CE}*

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Current paths through BJTs

Once the BJT's relative biasing voltage requirements are satisfied, if the base-emitter voltage (V_{BE}) on an NPN transistor is 0.6V, or -0.6V on a PNP transistor, the electrons move through the base-emitter junction toward the positive side of V_{BE}. This is shown in Figures 9a and 9b below.

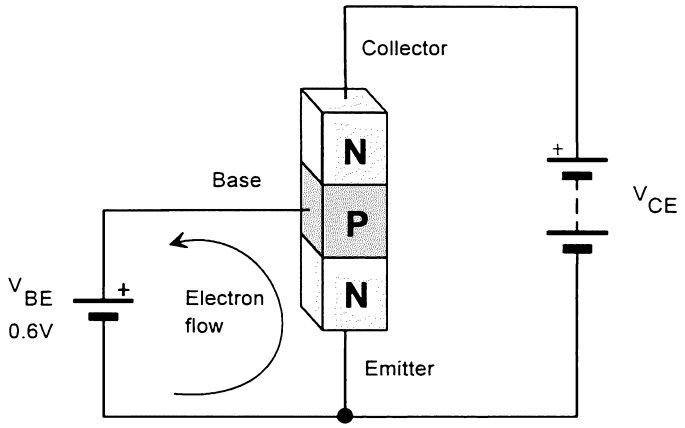

Figure 9a

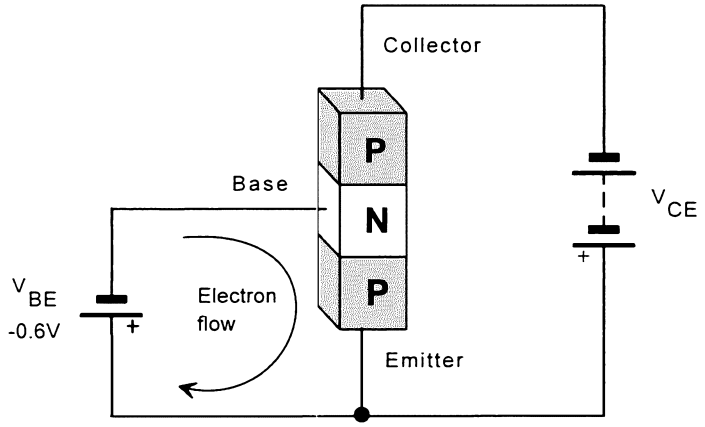

Figure 9b

Importantly, the layer of silicon for the base is actually very thin, so electrons going into it can't get out quickly enough. This causes an excess of electrons to build up in the base region until the base overflows and floods the depletion layer at the p-n junction between the base and collector. This allows electrons to move across the base-collector p-n junction even though it is reversed biased.

So, electrons travel via two paths through a BJT. One path is via the emitter and the base and the other via the emitter and the collector. These paths are shown in Figures 10a and 10b below.

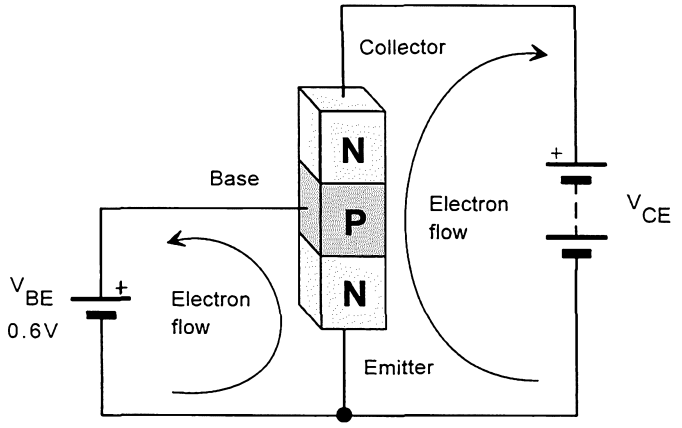

Figure 10a

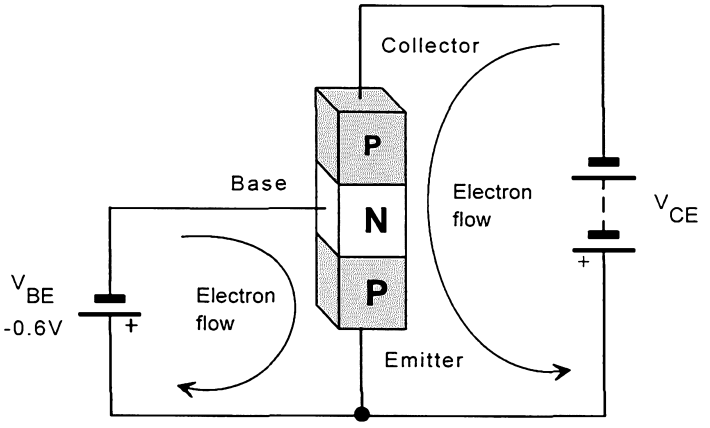

Figure 10b

Although our understanding of the BJT's operation relies on the movement of electrons, it is more common in this country to refer to conventional currents around a BJT and this is shown in Figures 11 and 12 below.

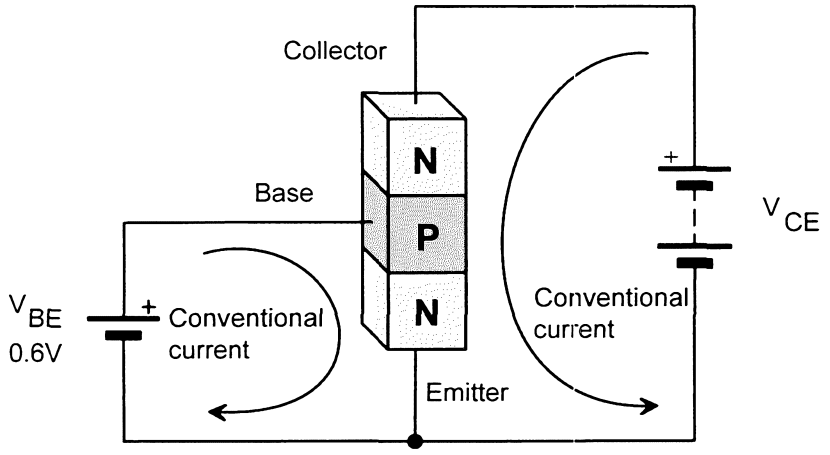

Figure 11 *The conventional currents flowing in the circuit of an NPN BJT with a V_{BE} of 0.6V*

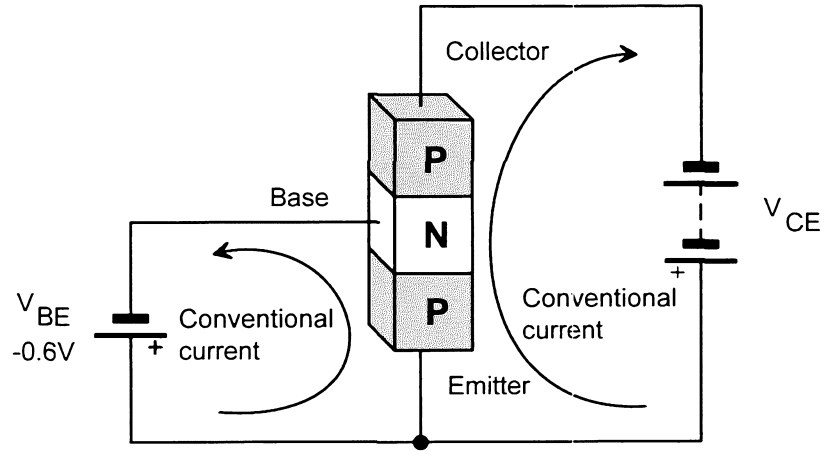

Figure 12 *The conventional currents flowing in the circuit of a PNP BJT with a V_{BE} of -0.6V*

If we show the direction of these currents using the schematic symbols for NPN and PNP BJTs we can see that the direction of conventional current in the emitter is indicated by the arrow head. This is shown in Figures 13a and 13b below.

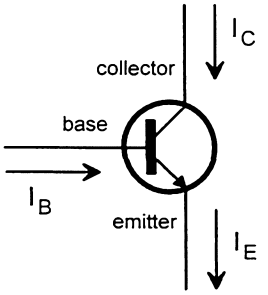

Figure 13a

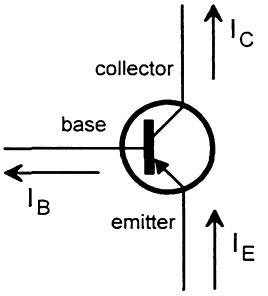

Figure 13b

These diagrams clearly show that both base and collector currents of BJTs flow through the emitter. So, the emitter current is the sum of the base and collector currents. This relationship can be expressed mathematically as:

$$I_E = I_B + I_C$$

Practise using this equation by trying the following questions.

1. What is the emitter current of an NPN BJT with a base current of 100μA and a collector current of 2mA?

   2.1 mA

2. What is the emitter current of a PNP BJT with a base current of 50μA and a collector current of 4.7mA?

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3. What is the base current of an NPN transistor with a collector current of 10mA and an emitter current of 10.095mA?

4. What is the collector current of a PNP BJT with a base current of 125μA and an emitter current of 2.45mA?

The relationship between base-emitter voltage and collector current in a BJT

If the relationship between the base-emitter voltage and collector current of an NPN BJT is measured and graphed, it would look like the graph in Figure 14 below (for PNP transistors, the graph would be the same but point to the left instead of the right).

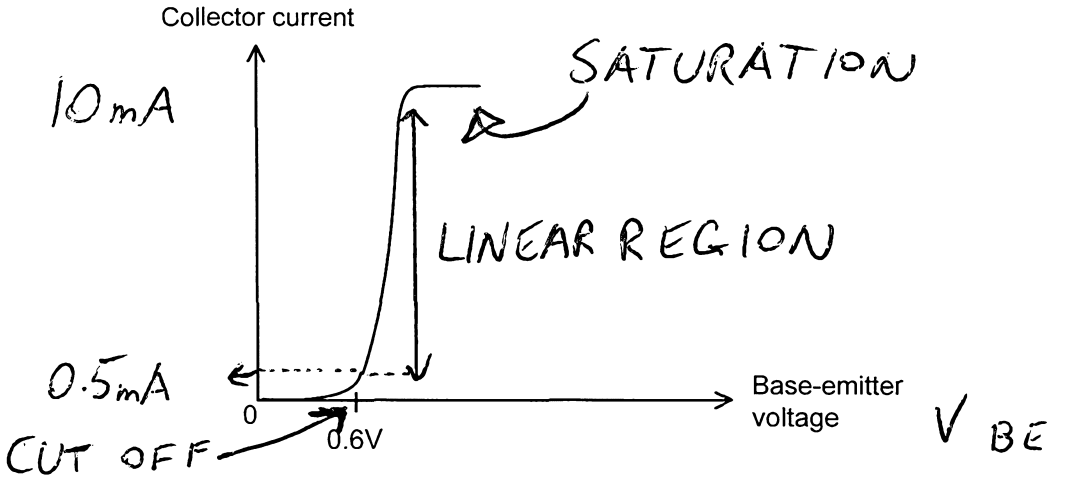

Figure 14 *The graph of base-emitter voltage versus collector current for an NPN BJT*

The relationship between the base and collector currents in a BJT

If the relationship between base and collector currents of an NPN BJT is measured and graphed, it would look like Figure 15 below (for PNP transistors, the graph would be the same but point to the left instead of the right).

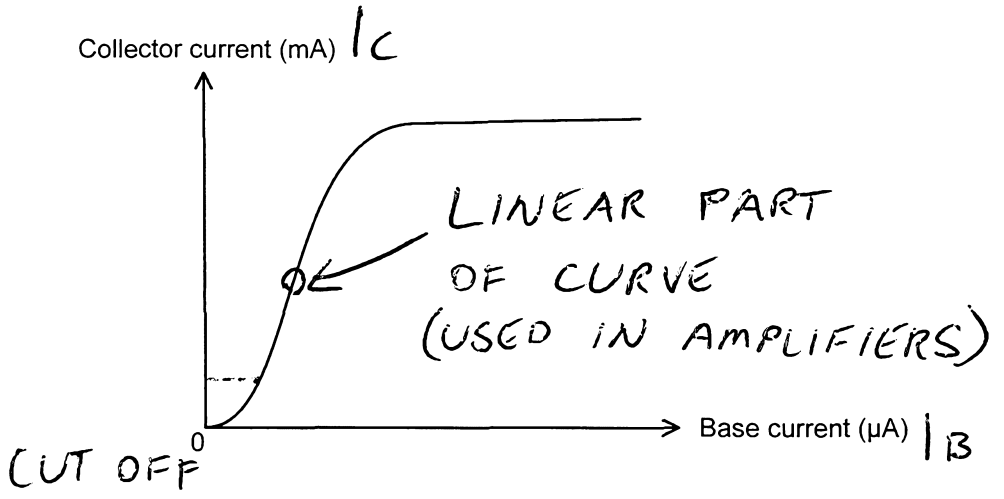

Figure 15 *The graph of base current versus collector current for an NPN BJT*

This graph highlights four important characteristics of BJTs. First, when there is no base current then there is no collector current. This is shown on the graph in Figure 16 and this condition is called *cut-off*.

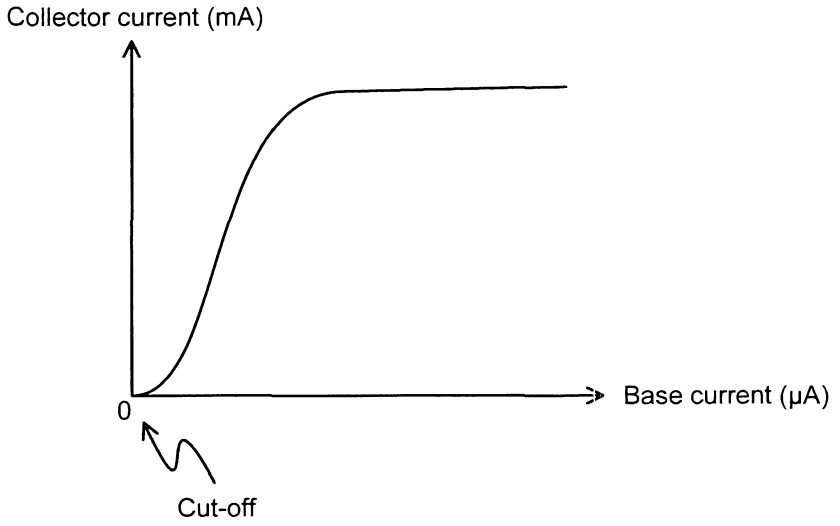

Figure 16 *The term "cut-off" is used to describe the BJT's condition when there is no collector current*

Second, when base current flows then collector current flows and these are proportional to each other. That is, as base current increases, collector current increases proportionally. This area on the graph of the BJT's base current versus collector current is called the "linear" region of operation and is shown on the graph in Figure 17. The BJT's operation discussed on this page is the reason for BJTs sometimes being referred to as "current-controlled" devices.

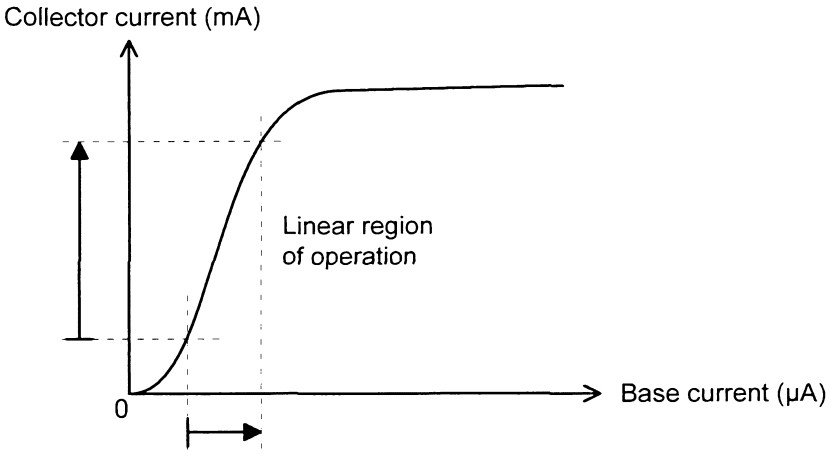

Figure 17 *As the base current increases, the collector current proportionally*

Third, the collector current is much bigger than the base current (notice on the graph that the base current is micro amps and the collector current is milli amps) and this is why the BJT is thought of as a current amplifier.

Fourth, although collector current increases as base current increases, it does so only up to a point. Once that point is reached, further increases in base current produce only very small changes in collector current. This condition is called *saturation* and is shown on the graph in Figure 18.

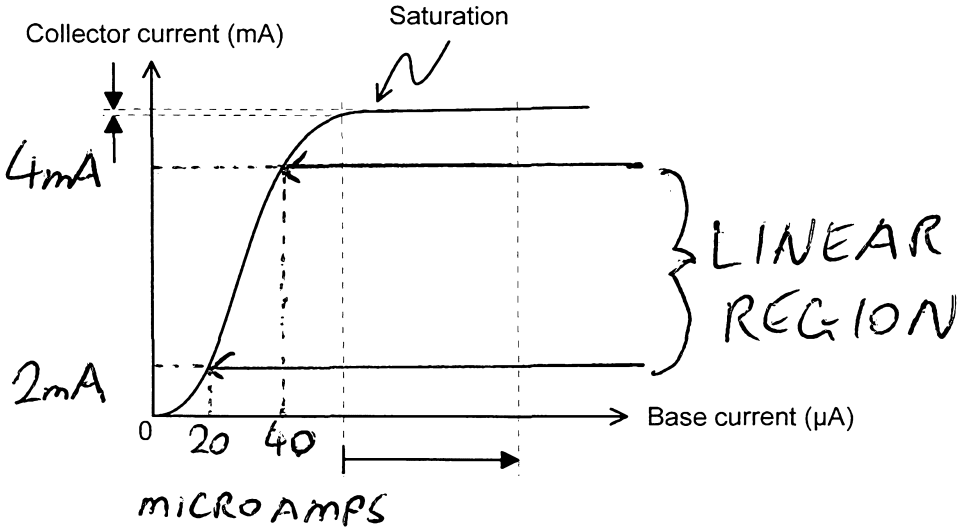

Figure 18 *When the transistor is saturated, further increases in base current result in only small increases in collector current*

Beta

As already mentioned, the BJT is a current amplifier and has a current gain. However, the current gain of BJTs is usually referred to as *beta*. Beta is represented by the Greek letter β but is also sometimes denoted as h_{FE} (strictly speaking, β and h_{FE} are not exactly the same but they're close enough for our purposes).

Recall that current gain is the ratio of output current to input current and for a BJT is calculated using the equation:

$$\beta = \frac{I_C}{I_B}$$

Where:
I_C is the collector current and
I_B is the base current

A transistor with a beta of 200 has a collector current that is 200 times greater than its base current when the device is forward biased. Typical values of beta range from 100 to 800 for small signal transistors and 20 to 150 for power transistors.

Practise using this equation by trying the following questions.

1. What is the beta (β) of an NPN BJT with a base current of 100μA and a collector current of 2mA?

2. What is the beta (β) of a PNP BJT with a base current of 50μA and a collector current of 4.7mA?

3. What is the collector current of a PNP transistor with a base current of 25μA and a beta (β) of 800?

4. What is the base current of a PNP transistor with a collector current of 1.7mA and a beta (β) of 390?

Summary

The operation of BJTs can be summarised as follows:

- BJTs are current amplifiers.
- If the base-emitter voltage (V_{BE}) is 0V, the BJT's base-emitter junction will not be forward biased. So, there'll not be a base current.
- If there is no base current then there'll be no collector current. This BJT condition is called cut-off.
- To forward bias the base-emitter junction, an NPN BJT needs a base-emitter voltage (V_{BE}) of 0.6V and a PNP BJT needs a base-emitter voltage of -0.6V.
- When the base-emitter junction of a BJT is forward biased, base current flows.
- Base current flows into the base of NPN BJTs and out of the base of PNP BJTs.
- When base current flows in a BJT, then collector current flows. For this reason, BJTs are sometimes referred to as "current-controlled" devices.
- Collector current flows into the collector of NPN BJTs and out of the collector of PNP BJTs.
- The collector current in a BJT will be bigger than the base current by a factor of beta (β).
- The base and collector currents in a BJT are proportional. That is, as base current goes up, collector current goes up. As base current goes down, collector current goes down.
- When the collector current can't go up any higher, the BJT is said to be saturated.
- The emitter current is the sum of the base and collector currents.
- Emitter current flows out of the emitter of NPN BJTs and into the emitter of PNP BJTs.

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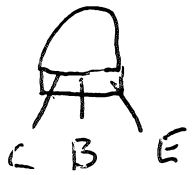
Student notes

BC549 TRANSISTOR:

- NPN TYPE
- PIN OUT: 1) COLLECTOR
  2) BASE
  3) EMITTOR



- SWITCH / AMP / LOW NOISE
- MAX VOLTAGE = 30V
- MAX CURRENT = 100mA
- CURRENT GAIN (H_{FE}) = 110 TO 800

Skill practice 1

Practise measuring DC currents in transistor circuits using a DMM

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 1 hour to complete this exercise.

Equipment

- prototyping panel
- three digital multimeters (DMMs)
- BD139 transistor
- 10kΩ ¼W resistor
- 1kΩ ¼W resistor
- 1MΩB (linear) pot
- banana leads
- hook-up wire
- wire strippers

Remember:

Follow TAFE NSW WHS guidance at all times!

Work tasks

1. Read your WHS responsibilities at the top of the form below. Then conduct a WHS risk assessment and record your findings in the space provided.

Responsibilities of students under the Model WHS Act: s28

- Take reasonable care for your own health and safety by working safely at all times
- Take reasonable care to ensure that your acts or omissions don't put the health and safety of others at risk
- Follow all TAFE NSW WHS guidance and comply with all reasonable instructions from TAFE NSW staff to assist them in complying with the TAFE NSW WHS requirements
- In addition to the above, you must:
  - use and maintain machinery, tools and all other equipment properly and safely
  - ensure that your work area is free of hazards
  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

Risks involved in this activity include:	**Control measures:**
Trip hazards (eg students bags) Objects dropped on feet (while equipment is taken to and from workbenches). Others: _____ _____ _____	Move bags and other objects from walkways Plan lifting of equipment Other: _____ _____ _____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

3. Adjust the bench-mounted power supply's right-side output for 10V DC then turn it off.

4. Wire the circuit of Figure 1.

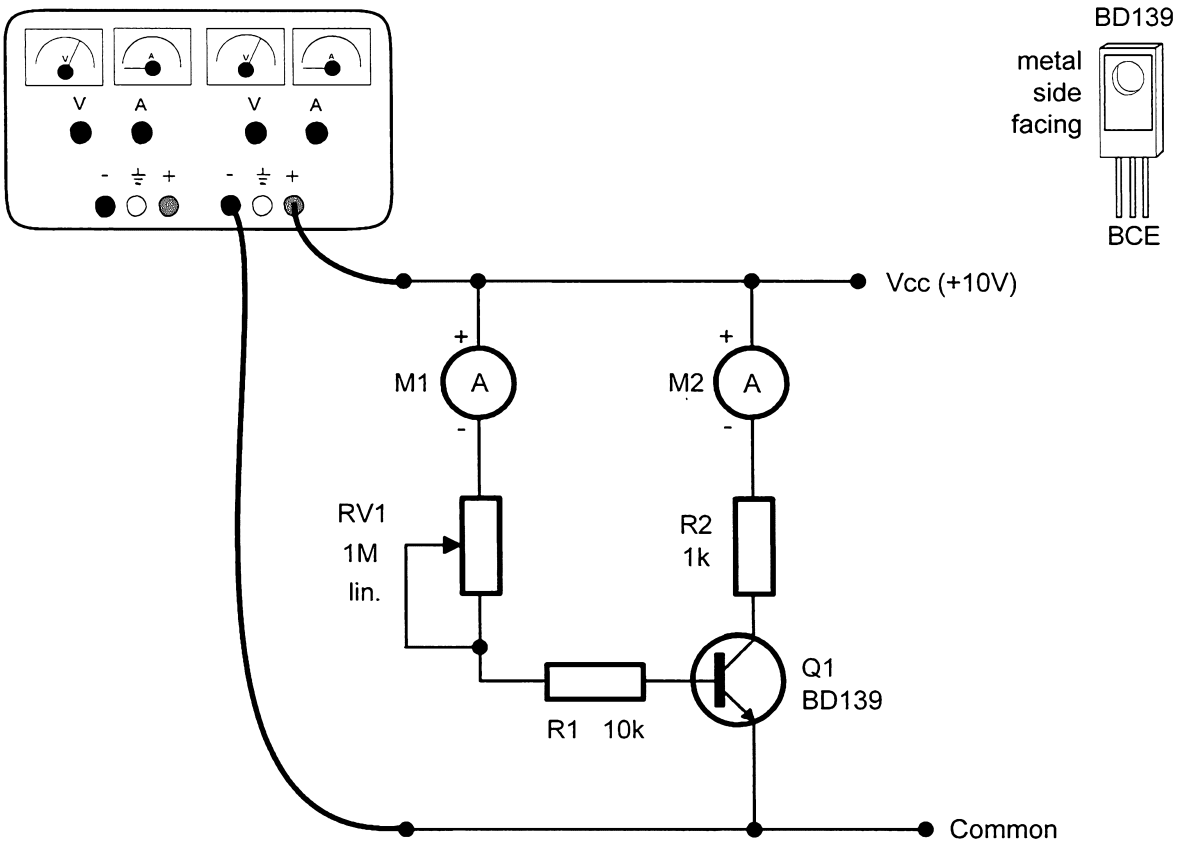


Figure 1

About the circuit
This circuit uses a single DC power supply to provide base current and collector current. A potentiometer is used to vary the base current which in turn varies the collector current and collector voltage. Meter M1 measures the base current and meter M2 measures the collector current. A third meter will be used to measure DC voltages around the circuit.

5. Set ammeters to the **mA** current range.

6. Switch on the power supply.

7. Measure the voltage on the base with respect to the circuit common. If the circuit is wired correctly you should measure 0.6V.

   If it's not 0.6V then turn off the power supply and check your wiring. If you can't find anything wrong, call the teacher.

8. Measure the voltage on the BJT's collector with respect to the circuit's common.

9. Turn the potentiometer's knob in both directions. If the circuit is wired correctly the collector voltage will vary.

   If the collector voltage doesn't vary then turn off the power supply and check your wiring. If you can't find anything wrong, call the teacher.

10. Adjust *RV1* so that the collector voltage is 8V.

11. Measure the potential difference across the collector resistor (*R2*). Record your measurements in Table 1 below.

12. Use meters M1 and M2 to measure the base and collector currents. Record your measurements in Table 1 also.

13. Use these measured currents to calculate and record the emitter current. If you're not sure how to do this, read the notes on page 1-13.

14. Use your measured currents to calculate and record the BJT's beta. Again, if you're not sure how to do this, read the notes on page 1-16.

Table 1		Collector at 8V	Collector at 3V
Measured (Steps 11 to 13)	**Potential difference across R2**	1.16 V	350 mV
	Base current (I_B)	8.5 µA	2.5 µA
	Collector current (I_C)	1.15 mA	350 mA
Calculated (Step 14)	**Emitter current (I_E)**	1.1585 mA	352.5 mA
	Beta (β)	135.3	140

The teacher needs to check your work at this point...

15. Adjust *RV1* so the collector voltage is 3V and repeat Steps 11 to 14.

Question 1
What is the typical beta of a power transistor? If you're not sure, see the bottom of page 1-17. Is your transistor's beta within specification?

8V = 135 ✓ Yes. Beta is within specification
3V = 140 (25-250)

Question 2
What does the *beta* tell us about a BJT?

Tells us about the current gain.

Question 3
What is the relationship between the base current and the collector current?

$I_C = \beta \times I_B$

Question 4
What is the relationship between the collector current and the collector voltage?

$V_C = V_{CC} - (I_C \times R_2)$

The teacher needs to check your work at this point...

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16. Simulate a fault in the circuit by removing resistor *R1* (but **don't** join the two points in the circuit that *R1* was connected to).

17. Measure the base and collector currents. Record your measurements in Table 2.

18. Measure and record the collector voltage.

Table 2

Base current (I_B)	**Collector current (I_C)**	**Collector voltage (V_C)**

Question 5
Why has the collector current fallen to zero?

Removing R1 stops the base current
The BJT can no loger turn on

Question 6
Why is the collector voltage now 10V?

Theres no voltge drop across R2
Therefore full Supply voltage appears at collector

Question 7
What is the term used to describe the operating condition the transistor is now in?

Cut off mode

The teacher needs to check your work at this point...

19. Put *R1* back in the circuit. Check M1 and M2 to make sure that the base and collector currents are flowing again.

20. Adjust *RV1* to set the transistor's base current to 0.025mA.

21. Measure the transistor's collector current. Record this current in Table 3 below.

22. Repeat steps 20 and 21 for all the base currents listed in Table 3

    Note: If the meter goes out of range then switch it to the next current range.

Table 3

Base current	Collector current
0.025mA	
.05mA	
0.1mA	
0.2mA	
0.4mA	
0.8mA	

Question 8
What is the relationship between the base current and collector current (for collector currents below approximately 10mA)?

_____

_____

Question 9
What happens to this relationship once the collector current exceeds approximately 10mA?

_____

_____

Question 10

What is the term used to describe the BJT's operating condition for this relationship between base and collector currents?

The teacher needs to check your work at this point...

Review questions

Answer these questions to check your understanding of what you have learnt for this chapter. Doing this will also help to prepare you for the tests.

1. Is a transistor a voltage amplifying device or a current amplifying device? Explain.

   _____

   _____

2. Which semiconductor material are most transistors made of? _____

3. How many terminals does a transistor have? _____

4. What are the two types of bipolar junction transistors? _____

5. Draw the schematic symbols for the two transistor types and label each one.

6. Label each lead of the transistor symbols you drew above.

7. Which leg of the transistor symbol has the *arrow*? _____

8. What does the arrow indicate the direction of? _____

9. Which of the two transistor types is better for high frequency circuits? _____

10. What is meant by the term *bias* with respect to transistors?

11. What is meant by the terms forward-bias and reverse-bias?

12. State whether the following p-n junctions are forward-biased or reverse-biased when both collector and base currents flow:

    base-emitter junction _____

    base-collector junction _____

13. What is the relationship between the emitter current and the collector and base currents?

14. A transistor has a current gain (beta) of 200. What does this tell about the relationship between its base current and collector current?

15. What is the current gain of a transistor with a base current of 50μA and a collector current of 12.5mA?

16. How much base current is needed to develop a collector current of 2mA if the transistor has a beta of 220?

17. What is the collector current of a transistor with a base current of 15μA and a beta of 310?

18. What is the beta of a transistor with a collector current of 1mA and an emitter current of 1.01mA?

19. How many volts would you expect to measure across a forward biased base-emitter junction?

20. What effect will increasing the base-emitter voltage of an NPN transistor have on its base current?

21. What effect will decreasing the base current of a transistor have on its collector current?

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22. What is meant by the term *cut-off* with respect to transistors?

23. What is meant by the term *saturation*?

Section 2 Transistor biasing circuits

Purpose To develop your knowledge and skills to help you locate amplifier faults by comparing predicted and measured DC voltages around two common BJT biasing circuits.

Objectives At the end of the lesson you should be able to:

- Recognise base biasing and voltage divider biasing BJT circuits in schematic diagrams
- Explain the function of each component in the base bias and voltage divider bias circuits
- Predict key DC voltages around the base bias and voltage divider bias circuits
- Measure key DC voltages around the base bias and voltage divider bias circuits and compare them to predicted values
- Explain why measured DC voltages are unlikely to be exactly the same as calculated values

Introduction

The last chapter introduced you to BJT biasing requirements using an oversimplified circuit. In this section you'll examine the operation of two practical and commonly used methods of biasing a BJT; base bias and voltage divider bias (there are other bias methods but you'll be introduced to them later in this subject).

But first, you must be able to distinguish between the two ways that voltages around transistor circuits can be expressed.

Voltage measurements

There are two ways of expressing and measuring voltages around transistor circuits:

- **With respect to common:** The meter's black probe is connected to the circuit's common line and its red probe is connected to the point to be measured. This is how most DC voltages are measured and how nearly all CRO measurements are made.

- **Potential difference between two points:** The meter's black probe is connected to one point in the circuit (other than common) and its red probe is connected to another. This type of measurement cannot be made using a CRO (and it's unnecessary too).

Because there are two ways of expressing and measuring voltages around a BJT circuit, we need to be able to distinguish between them when writing them down.

If a voltage is written as "V_X" then it's understood that it is the voltage at point X measured with respect to common. That is, the meter's red probe was connected to point X in the circuit and its black probe was connected to common.

If a voltage is written as V_{XY} then it's the voltage at point X measured with respect to point Y. That is, the meter's red probe was connected to point X in the circuit and its black probe was connected to point Y.

The list below shows the six ways that the voltages on the leads of a BJT can be measured in a circuit:

$\mathbf{V_C}$ voltage at the collector with respect to common

$\mathbf{V_B}$ voltage at the base with respect to common

$\mathbf{V_E}$ voltage at the emitter with respect to common

$\mathbf{V_{CE}}$ voltage at the collector with respect to the emitter

$\mathbf{V_{CB}}$ voltage at the collector with respect to the base

$\mathbf{V_{BE}}$ voltage at the base with respect to the emitter

As with circuits you have learnt about in other modules, it is possible to measure the potential difference across individual components. Such measurements are written as V_{ZZ} *where* ZZ is the abbreviation for the component's name. For example:

$\mathbf{V_{RC}}$ potential difference across the collector resistor

$\mathbf{V_{RE}}$ potential difference across the emitter resistor

$\mathbf{V_{RB}}$ potential difference across the base resistor

$\mathbf{V_{RB1}}$ potential difference across the base resistor R_{B1}

$\mathbf{V_{RB2}}$ potential difference across the base resistor R_{B2}

There are also abbreviations for the power supply rails. Commonly used abbreviations include:

$\mathbf{V_{CC}}$ a supply rail in BJT circuits (usually positive but not always)

$\mathbf{V_{EE}}$ a supply rail in BJT circuits (usually negative but not always)

$\mathbf{V_{DD}}$ a supply rail in FET circuits (usually positive but not always)

$\mathbf{V_{SS}}$ a supply rail in FET circuits (usually negative but not always)

Transistor biasing circuits

There are several biasing circuits for the BJT. This workbook introduces you to two of them:

- Base bias
- Voltage divider bias

Base bias (also known as Fixed bias)

Figure 1 below shows a base biased BJT amplifier circuit using an NPN transistor. Notice that only one power supply is used and it provides all of the BJT's biasing needs. Notice also that the point in the circuit that is connected to the power supply's negative terminal is called *common*. The reason it is so called is explained in the next section but, at this point, it is important to know that it's the circuit's 0V reference.

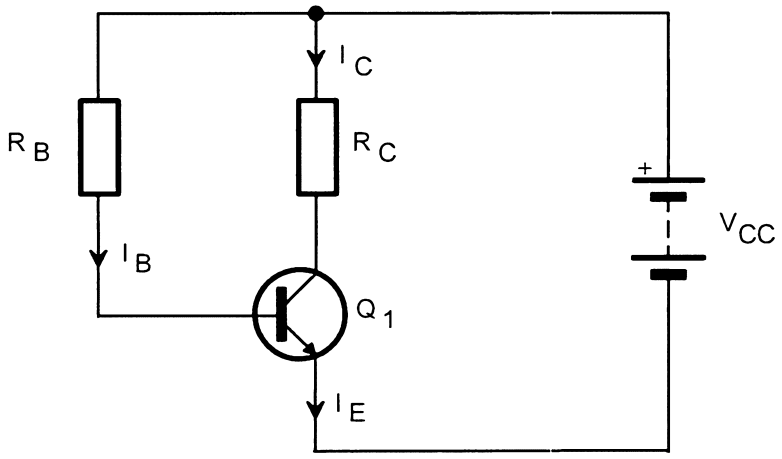

Figure 1 *Base bias circuit showing current paths and relevant voltages*

How the biasing works

As the base is connected to the supply (V_{CC}) via the base resistor (R_B) its voltage is more positive than the emitter. So the base-emitter junction is forward biased. That being the case, base current (I_B) flows from the supply voltage to common via the base resistor (R_B) and through base-emitter junction.

As the there is a base current, collector current (I_C) also flows. It travels via the collector resistor (R_C) into the transistor's collector and out of its emitter leg to common.

(Importantly, the current through R_C develops a potential difference across it (V_{RC}) that causes the transistor's collector voltage with respect to common (V_C) to be a value below the supply voltage. Care in the choice of the value of R_C is needed to ensure that V_C is a value that is above V_B to obtain the junction biasing conditions necessary for NPN BJTs.)

The function of each component in the circuit is as follows:

- The power supply (V_{CC}) provides DC power to the circuit and provides all the necessary biasing voltages.
- The base resistor (R_B) provides a path from the supply for base current to flow. At the same time, the resistor sets the amount of base current that flows.
- The transistor (Q_1) amplifies the base current and produces a larger collector current.
- The collector resistor (R_C) provides a path for the collector current to flow. It also sets up the quiescent (or "steady state") DC collector voltage (V_C) and converts changes in collector current to changes in collector voltage.

Testing base bias circuits

Electronics technicians are expected to be able to repair electronics equipment consisting of BJT amplifier circuits. This means that you'll need to be able to determine whether these circuits are working or not. As most faults cause changes in the quiescent DC voltages around the circuit, testing the circuit involves:

1. Measuring key DC circuit voltages;
2. Calculating the voltages (if they're not provided on the schematic diagram); then
3. Comparing the measured and calculated voltages.

   If the measured and calculated voltages are the same or similar then the circuit is probably working. If they're not the same then there may be a problem.

The key circuit voltages in a base bias circuit are: the voltage on the BJT's collector terminal relative to common (V_C); and the voltage on the BJT's base terminal relative to common (V_B). How to measure these voltages is shown in Figures 2a and 2b on the next page.

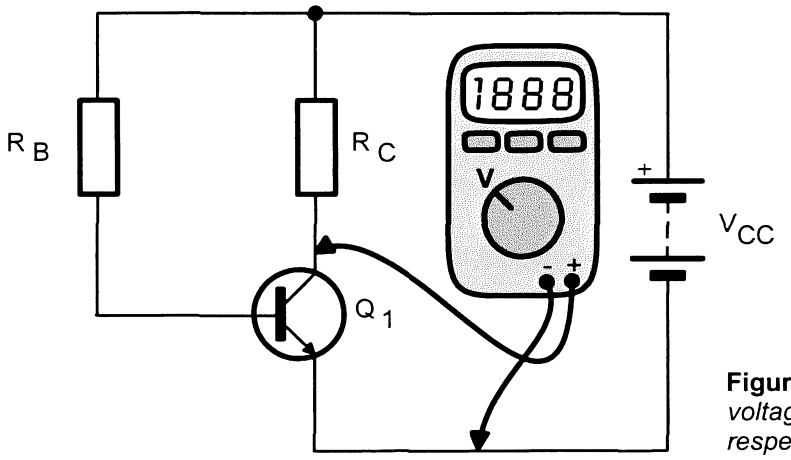

Figure 2a *Measuring the voltage on the collector with respect to common (V_C)*

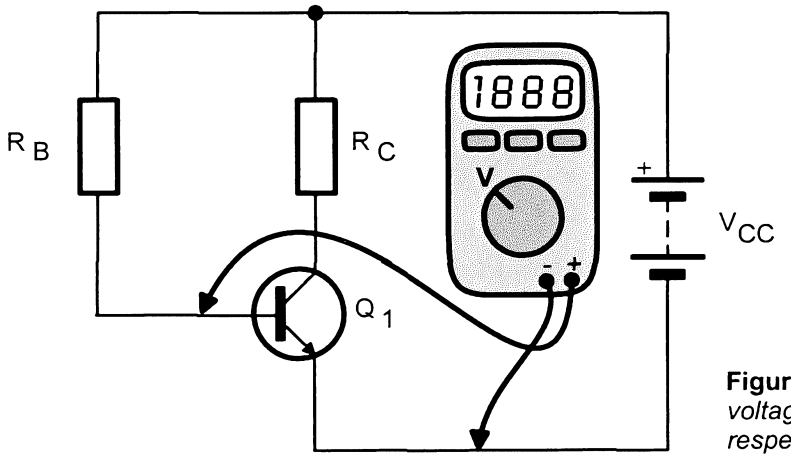

Figure 2b *Measuring the voltage on the base with respect to common (V_B)*

Once you have measured these voltages, the next step is to work out what they should be. How this is done for the base bias circuit is shown on the next page.

Calculations

To calculate the base voltage of the base bias circuit:

Find V_B Recall that the connection between the base and the emitter of a BJT is a p-n junction. Recall also that, when a p-n junction is forward biased, its potential difference is 0.6V. And, as the emitter is connected to common (which is 0V), then:

$V_B = 0.6V$ for NPN

$V_B = -0.6V$ for PNP

Calculating the collector voltage is a three-step process:

1. Find I_B The base current is set by the base resistor and is found by dividing the potential difference across the resistor by its resistance (Ohm's Law). As the voltage on either side of R_B is known, the base current can be found using the equation:

$$I_B = \frac{V_{CC} - V_B}{R_B}$$

2. Find I_C Recall from the theory in Section 1, the collector current is bigger than the base current by a factor of beta.

$$I_C = \beta \times I_B$$

3. Find V_{RC} Ohm's Law can be used to calculate the potential difference across the collector resistor:

$$V_{RC} = I_C \times R_C$$

4. Find V_C Kirchhoff's Voltage Law tells us that the collector voltage (with respect to common) is equal to the supply voltage minus the potential difference across the collector resistor.

$$V_C = V_{CC} - V_{RC}$$

It's important to note here that, even if the circuit is working correctly, it's likely that the measured and calculated base and collector voltages will be a little different. There are three reasons for this:

- Resistors have tolerances (typically ±5%)
- The forward voltage drop of the base-emitter junction is not exactly 0.6V (it can vary from 0.5V to 0.7V)
- The beta of BJTs varies from one to another (for example, the range of beta for a BC549 is 110 to 800!)

There are two other potential differences in the base bias circuit that can be calculated and these are: the voltage on the collector relative to the emitter (V_{CE}); and the voltage on the collector relative to the base (V_{CB}).

It is important to stress here that you're probably unlikely to measure these voltages when testing BJT amplifier circuits. This is because the experienced technicians are able to work out whether the circuit is probably working by measuring only V_B and V_C.

So why calculate V_{CE} and V_{CB}? In your work you'll find that it's often difficult to replace faulty components with original parts. This can be especially true of transistors. Later in this subject we'll look at how to choose suitable substitutes for transistors that you can't track down. To be able to do so often requires you to be able to calculate the potential differences across the collector-emitter and collector-base so this is dealt with here.

Find V_{CE} The voltage at the collector with respect to the emitter is found by simply subtracting the emitter voltage from the collector voltage.

$$V_{CE} = V_C - V_E$$

Find V_{CB} The voltage at the collector with respect to the base is found by simply subtracting the base voltage from the collector voltage.

$$V_{CB} = V_C - V_B$$

Practise calculating the voltages around the circuit of base biased BJTs by trying the following questions.

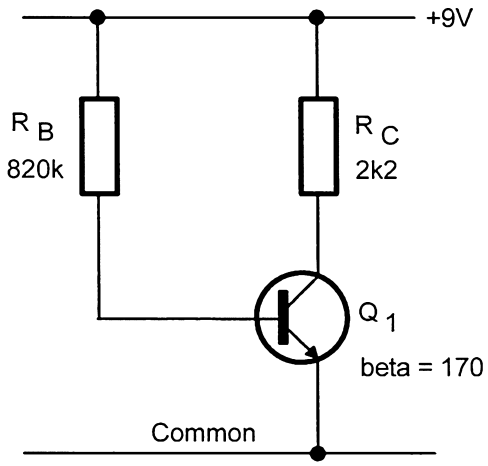

Figure 3

1. Calculate the base voltage (V_B) of the circuit in Figure 3.

2. Calculate the base current (I_B).

3. Calculate the collector current (I_C).

4. Calculate the collector voltage (V_C).

5. Calculate the collector-emitter voltage (V_{CE}).

6. Calculate the collector-base voltage (V_{CB}).

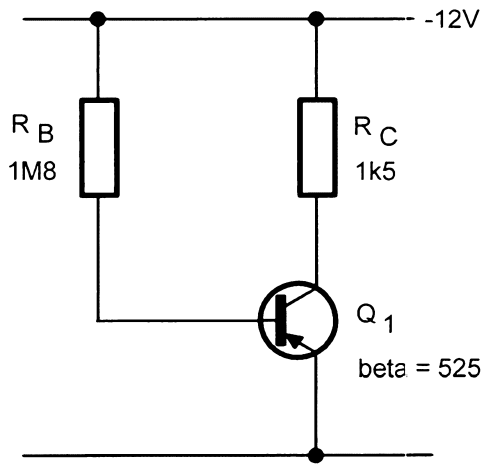

Figure 4

7. Calculate the base voltage (V_B) of the circuit in Figure 4.

8. Calculate the base current (I_B).

9. Calculate the collector current (I_C).

10. Calculate the collector voltage (V_C).

11. Show on Figure 4 the direction of the PNP transistor's three currents.

Note: When analysing real circuits, the resistors are not going to be labelled R_B and R_C. Instead, they'll be labelled something like *R56* and *R57*. That being the case, you'll have to identify which resistor in the circuit is the base resistor and which is the collector resistor and use their values in these equations.

Limitations of base bias

The base bias configuration is not very stable because even small changes in the transistor's beta due to heat or age can cause changes in the quiescent DC conditions in part of the circuit and, in turn, risks upset its operation. The same problem arises if the transistor is replaced for another with a different beta.

To demonstrate these problems, let's consider what happens to the circuit in Figure 3 if the BJT is replaced with another having a beta (β) of 350.

First, the base voltage remains 0.6V and so the potential difference across the base resistor and the base current don't change. However, the collector current changes because the beta is now 350. The new collector current is 3.58mA which means that the collector voltage drops to 1.11V. This is substantially different to the circuit's collector voltage that you calculated in question 4 and, as you will read in the next section, it would also upset the circuit's AC operation.

Other base bias circuits

Although the example of the base bias NPN BJT circuit discussed earlier uses a positive supply rail, it's possible to operate the device in a base bias circuit with a negative supply. Similarly, it's possible to operate the PNP BJT in a base bias circuit with a positive supply. Examples and their analysis are provided in Appendix 1.

Voltage divider bias (also known as Combination bias)

Figure 5 below shows the circuit of a voltage divider biased BJT amplifier using an NPN transistor.

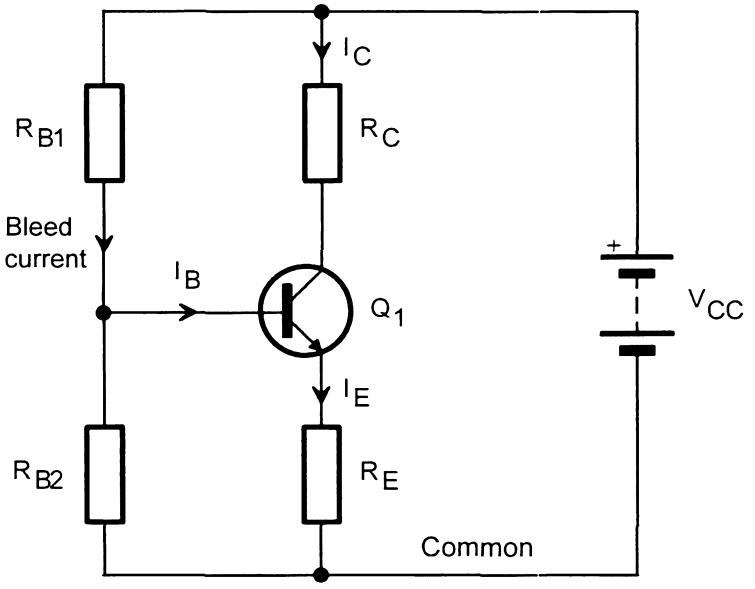

Figure 5 *The voltage divider bias circuit*

This biasing method is much more stable than the base bias circuit because the emitter resistor (R_E) introduces negative feedback which makes the bias conditions independent of beta (as long as the BJT's beta is sufficiently high). This is similar to the way the voltage gain of closed-loop op-amp circuits is independent of the op amp's open-loop gain.

Here's how the biasing works

Base resistors R_{B1} and R_{B2} form a voltage divider and current flows from the supply to common both resistors. This is called the *bleed current* . Recall from Kirchhoff's Voltage Law that the supply voltage is divided between the resistors and so R_{B2} has a potential difference across it that makes the BJT's base voltage bigger than 0V but less than *Vcc*.

If the potential difference across R_{B2} is greater than 0.6V, the BJT's base-emitter p-n junction is forward biased and a small amount of the bleed current branches off and travels to common via the base-emitter junction and the emitter resistor. This branch current is the transistor's base current (I_B).

As there is a base current, collector current (I_C) also flows. It travels via the collector resistor into the transistor's collector and out of its emitter terminal, through the emitter resistor to common.

(Again, R_C must be a value that ensures that V_C is a value that is above V_B to obtain the junction biasing conditions necessary for NPN BJTs.)

The function of each component in the circuit is as follows:

- The power supply (V_{CC}) provides DC power to the circuit and provides all the necessary biasing voltages.
- The base resistors (R_{B1} and R_{B2}) set up a fixed voltage on the base and provide a path from the supply for base current to flow.
- The transistor (Q_1) amplifies the base current and produces a larger collector current.
- The emitter resistor (R_E) sets the amount of emitter current (I_E) in the circuit. Also, as mentioned earlier, R_E provides negative feedback to the circuit. How this is done is explained later in this subject.
- The collector resistor (R_C) provides a path for the collector current to flow. It also sets up the quiescent DC collector voltage (V_C) and converts changes in collector current to changes in collector voltage.

Testing voltage divider biased BJT circuits

The procedure for testing base bias circuits is also used to test voltage divider biased circuits. You measure key voltages around the circuit and compare them to given or predicted values.

The key circuit voltages that you need to check are: the voltage on the BJT's collector terminal relative to common (V_C); the voltage on the BJT's base terminal relative to common (V_B); and the voltage on the BJT's emitter terminal relative to common (V_E). How to measure these voltages is shown in Figure 6a below and Figures 6b and 6c on the next page.

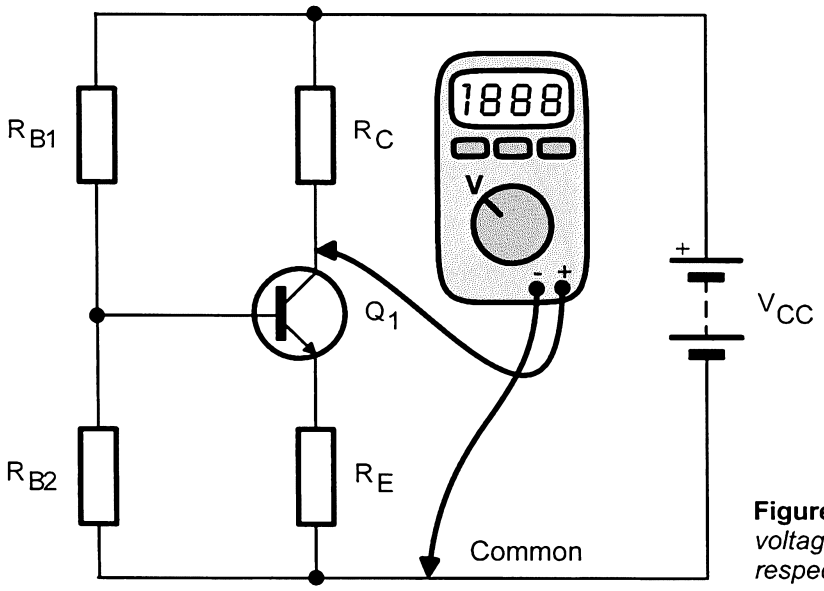

Figure 6a *Measuring the voltage on the collector with respect to common (V_C)*

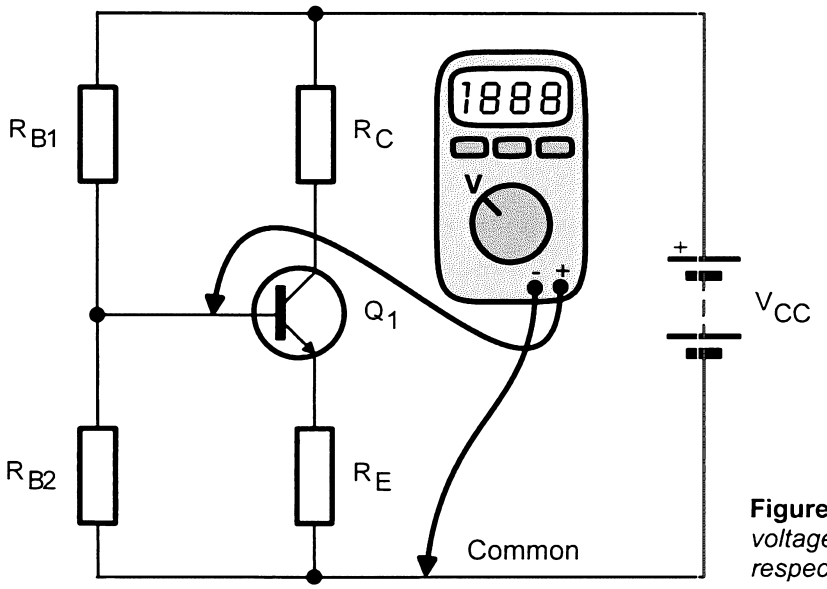

Figure 6b *Measuring the voltage on the base with respect to common (V_B)*

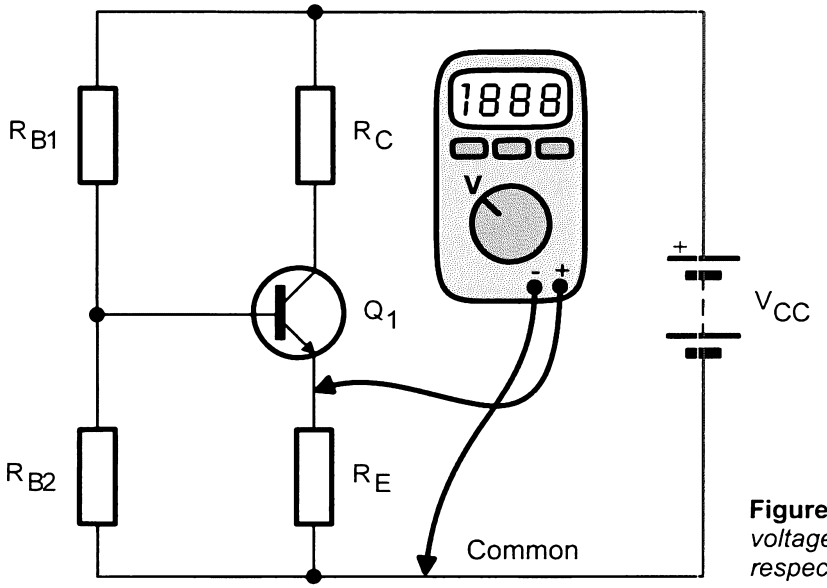

Figure 6c *Measuring the voltage on the emitter with respect to common (V_E)*

Once you've measured these voltages, the next step is to work out what they should be. How this is done for the voltage divider bias circuit is shown on the next page.

Calculations

The starting point for calculating the voltages on the pins of the BJT in the voltage divider bias circuit is the voltage on the base.

Find V_B The base voltage is calculated by using the voltage divider equation:

$$V_B = V_{CC} \times \frac{R_{B2}}{R_{B1}+R_{B2}}$$

Using the base voltage, we can calculate the emitter voltage:

Find V_E As you know, there is a 0.6V potential difference across the base-emitter junction when the BJT is forward biased. So, the emitter voltage is:

$V_E = V_B - 0.6V$ for NPN

$V_E = V_B + 0.6V$ for PNP

Finally, once the emitter voltage is known, the collector voltage can be found and this is a three-step process.

1. Find I_C As the base current is so small, the collector current is virtually the same as the emitter current. So, the collector current can be found by calculating the emitter current. This is done using Ohm's Law as shown below:

$$I_C \approx I_E = \frac{V_E}{R_E}$$

2. Find V_{RC} Ohm's Law can be used to calculate the potential difference across the collector resistor R_C.

$$V_{RC} = I_C \times R_C$$

3. Find V_C The collector voltage is found using the same equation as for the base bias circuit.

$$V_C = V_{CC} - V_{RC}$$

Again, even if the circuit is working correctly, it's likely that the measured and calculated base, collector and emitter voltages will be a little different. There are two reasons for this:

- Resistors have tolerances (typically ±5%)
- The forward voltage drop of the base-emitter junction is not exactly 0.6V (it can vary from 0.5V to 0.7V)

Note: Variations in beta between BJTs wont affect the DC voltages around the voltage divider bias circuit because, as mentioned earlier, they're independent of beta (due to negative feedback).

To assist when choosing suitable substitutes when replacing the BJT it is necessary to be able to calculate the collector-emitter voltage (V_{CE}) and the collector-base voltage (V_{CB}) of the circuit. These can be calculated in the same way as for the base bias circuit (see page 2-8).

Practise calculating the voltages around the circuit of voltage divider biased BJTs by trying the following questions.

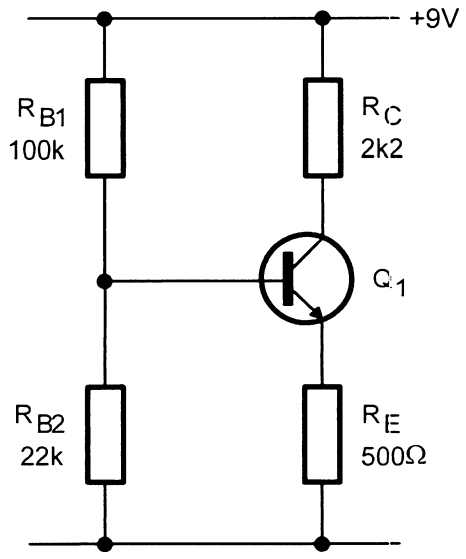

Figure 7

1. Calculate the base voltage (V_B) of the circuit in Figure 7.

2. Calculate the emitter voltage (V_E).

3. Calculate the collector current (I_C).

4. Calculate the collector voltage (V_C).

5. Calculate the collector-emitter voltage (V_{CE}).

6. Calculate the collector-base voltage (V_{CB}).

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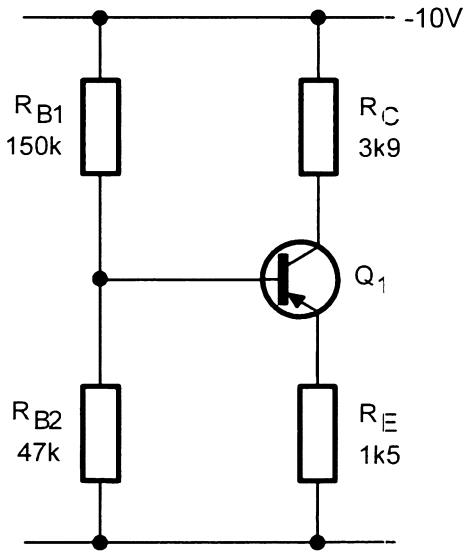

Figure 8

7. Calculate the base voltage (V_B) of the circuit in Figure 8.

8. Calculate the emitter voltage (V_E).

9. Calculate the collector current (I_C).

10. Calculate the collector voltage (V_C).

11. Show on Figure 8 the direction of the PNP transistor's three currents.

Note: When analysing real circuits, the resistors are not going to be labelled R_{B1}, R_{B2}, R_C and so on. Instead, they'll be labelled something like *R104*, *R105* and so on. That being the case, you'll have to identify which resistor in the circuit is which and use their values in these equations.

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Student notes

Skill practice 2

Practise measuring DC voltages in BJT amplifiers using a DMM

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 1¼ hours to complete this exercise.

Equipment

- Emona Trainer
- DMM
- BC549 transistor (or equivalent)
- 82kΩ ¼W resistor
- 22kΩ ¼W resistor
- 33kΩ ¼W resistor
- 6k8Ω ¼W resistor
- two 4k7Ω ¼W resistors
- 1k5Ω ¼W resistor
- hook-up wire
- wire strippers

Remember:

Follow TAFE NSW WHS guidance at all times!

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Work tasks

1. Read your WHS responsibilities at the top of the form below. Then conduct a WHS risk assessment and record your findings in the space provided.

Responsibilities of students under the Model WHS Act: s28

- Take reasonable care for your own health and safety by working safely at all times
- Take reasonable care to ensure that your acts or omissions don't put the health and safety of others at risk
- Follow all TAFE NSW WHS guidance and comply with all reasonable instructions from TAFE NSW staff to assist them in complying with the TAFE NSW WHS requirements
- In addition to the above, you must:
  - use and maintain machinery, tools and all other equipment properly and safely
  - ensure that your work area is free of hazards
  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

Risks involved in this activity include:	**Control measures:**
Trip hazards (eg students bags) Objects dropped on feet (while equipment is taken to and from workbenches).	Move bags and other objects from walkways Plan lifting of equipment
Others: _____	Other: _____
_____	_____
_____	_____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

3. Make sure the Emona Trainer is turned off.

4. Wire the circuit of Figure 1.

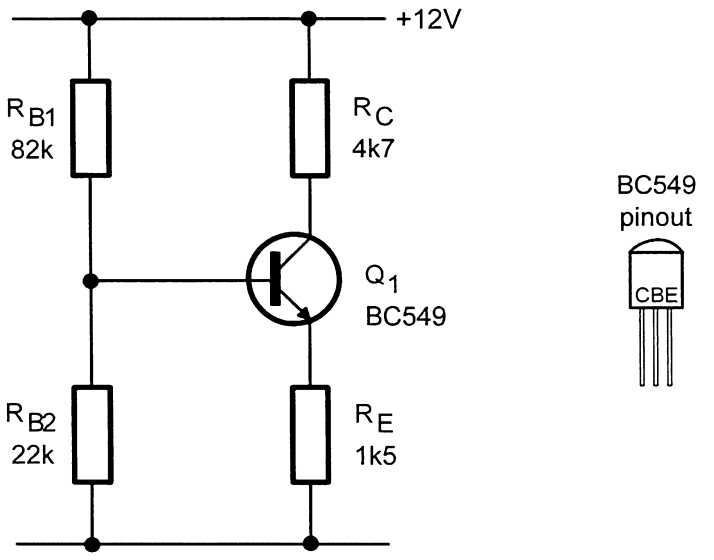

Figure 1

5. Switch on the Emona Trainer.

6. Measure the base-emitter voltage (V_{BE}). To do this, connect the meter's black probe to the BJT's emitter lead and the red probe to the base lead.

   Self-check: If the circuit is working the meter should read a voltage between 0.55V and 0.7V. If this is what you measure then jump to Step 9 (on the next page).

7. If you don't measure a base-emitter voltage of between 0.55V and 0.7V then there is something wrong. Turn off the Emona Trainer and check your wiring.

8. Once you have checked your wiring and made any necessary changes, turn on the DC power supply and check the base-emitter voltage again. If the base-emitter voltage is still not right then turn off the Emona Trainer and call the teacher.

9. Calculate the voltage on the transistor's base (V_B) . Record this in Table 1 below. (Note: If you're not sure how to calculate V_B, read the notes on voltage divider bias in this chapter.)

10. Measure and record the base voltage with respect to common using the DMM. Your calculated and measured results should be similar. If they're not, call the teacher.

Table 1 - Base voltage

Calculated (Step 9)	**Measured** (Step 10)

11. Calculate the voltage on the transistor's emitter (V_E). Record this in Table 2 below. (Again, if you are not sure how to calculate this value, read the notes.)

12. Measure and record the emitter voltage with respect to common using the DMM.

Table 2 - Emitter voltage

Calculated (Step 11)	**Measured** (Step 12)

13. Calculate the transistor's collector current (I_C). Record this in Table 3 below.

14. Measure and record the collector current. **Before** you do, read the two important points that follow:

    a) Make sure the meter is set for measuring current on the mA range and the meter's red lead is plugged in the DMM's correct socket.

    b) To measure the collector current, you'll have to break the circuit and connect the ammeter in series with the collector resistor.

Table 3 - Collector current

Calculated (Step 13)	**Measured** (Step 14)

15. Calculate the potential difference across the collector resistor (V_{RC}) using the equation $V_{RC} = I_C \times R_C$. Record this in Table 4 below.

16. Readjust the meter for measuring DC volts then measure and record the potential difference across the collector resistor.

Table 4 - Potential difference across R_C

Calculated (Step 15)	Measured (Step 16)

17. Calculate the BJT's collector voltage (V_C). Record this in Table 5 below.

18. Measure and record the collector voltage with respect to common.

Table 5 - Collector voltage

Calculated (Step 17)	Measured (Step 18)

Question 1
Give two reasons for your measured and calculated voltages not being exactly the same?

_____

_____

Question 2
What is the relationship between the potential difference across the collector resistor (see Table 4), the collector voltage (see Table 5) and the power supply voltage?

_____

_____

The teacher needs to check your work at this point...

19. Simulate the resistor R_{B2} having gone high in value by substituting it for a 33kΩ resistor.

20. Measure the base, emitter and collector voltages (with respect to common as you did earlier). Record your measurements in Table 6 below.

Table 6

Base voltage (V_B)	
Emitter voltage (V_E)	
Collector voltage (V_C)	

Question 3
Why did increasing the value of R_{B2} cause the base voltage to go up?

Question 4
Why did this cause the emitter voltage to go up?

Question 5
Why did this cause the collector voltage to go down?

The teacher needs to check your work at this point...

21. Return R_{B2} to a 22kΩ resistor.

22. Simulate the emitter resistor (R_E) having gone high by substituting it for a 4k7Ω resistor.

23. Measure the base, emitter and collector voltages recording them in Table 7 below.

Table 7

Base voltage (V_B)	
Emitter voltage (V_E)	
Collector voltage (V_C)	

Question 6
Why didn't increasing the value of the emitter resistor (R_E) have any effect on the base voltage?

_____

_____

Question 7
Why didn't increasing the value of R_E have any effect on the emitter voltage?

_____

_____

Question 8
If the emitter voltage didn't change, why did the collector voltage go up?

_____

_____

The teacher needs to check your work at this point...

24. Return R_E to a 1k5Ω resistor.

25. Simulate the collector resistor (R_C) having gone high by substituting it for a 6k8Ω resistor.

26. Measure the base, emitter and collector voltages recording them in Table 8 below.

Table 8

Base voltage (V_B)	
Emitter voltage (V_E)	
Collector voltage (V_C)	

Question 9
Why did increasing the value of the collector resistor (R_C) cause the collector voltage to go down?

_____

_____

Question 10
Why did increasing the value of R_C have no effect on the base and emitter voltages?

_____

_____

The teacher needs to check your work at this point...

27. Return R_C to a 4k7Ω resistor.

28. Simulate the transistor's base-emitter junction having gone short-circuit by using a piece of hook-up wire to connect them together.

29. Measure the base, emitter and collector voltages recording them in Table 9 below.

Table 9

Base voltage (V_B)	
Emitter voltage (V_E)	
Collector voltage (V_C)	

Question 11
Why did shorting the transistor's base-emitter junction cause the base voltage to go down?

_____

_____

Question 12
Why did shorting the base-emitter junction cause the collector voltage to rise to 12V?

_____

_____

The teacher needs to check your work at this point...

30. Remove the hook-up wire shorting the transistor's base-emitter junction.

31. Simulate the transistor's collector-emitter junction having gone short-circuit by using a piece of hook-up wire to connect them together.

32. Measure the base, emitter and collector voltages recording them in Table 10 below.

Table 10

Base voltage (V_B)	
Emitter voltage (V_E)	
Collector voltage (V_C)	

Question 13
Why did shorting the transistor's collector-emitter junction cause the collector voltage to go down instead of causing the emitter voltage to go up?

The teacher needs to check your work at this point...

Review questions

Answer these questions to check your understanding of what you have learnt for this chapter. Doing this will also help to prepare you for the tests.

Questions 1 to 9 refer to the circuit in Figure 1

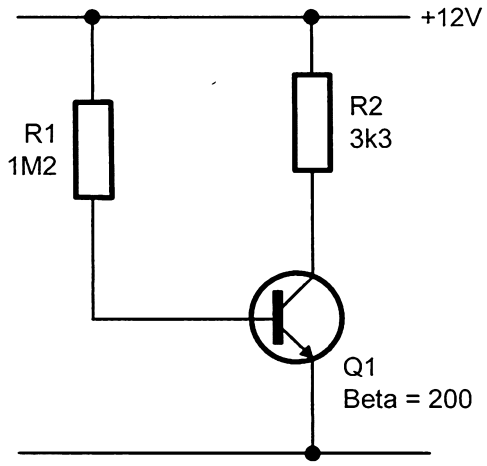

Figure 1

1. What biasing method does the circuit use?

_____

2. In which direction does the collector current flow?

   ☐ Into the emitter and out of the collector
   ☐ Into the collector and out of the emitter
   ☐ Into the collector and out of the base

3. In which direction does the base current flow?

   ☐ Into the emitter and out of the base
   ☐ Into the base and out of the collector
   ☐ Into the base and out of the emitter

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4. Calculate the base voltage.

5. Calculate the base current.

6. Calculate the collector current.

7. Calculate the collector voltage.

8. What would happen to the collector voltage if the transistor was substituted for a BJT with a higher beta? Explain your answer.

9. Can the BJT be substituted for a PNP BJT with equivalent specifications? Explain your answer.

Questions 10 to 16 refer to the circuit in Figure 2

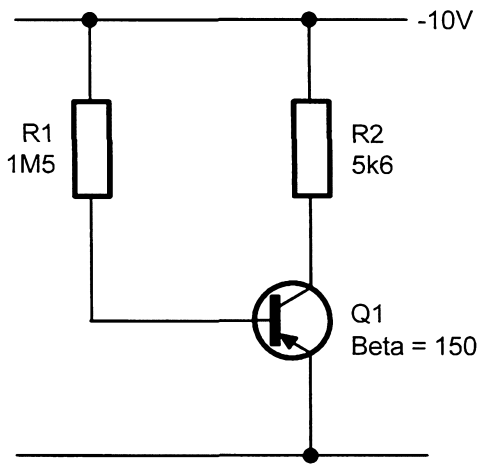

Figure 2

10. What biasing method does the circuit use?

_____

11. In which direction does the collector current flow?

- ☐ Into the emitter and out of the collector
- ☐ Into the collector and output of the base
- ☐ Into the collector and out of the emitter

12. In which direction does the base current flow?

- ☐ Into the emitter and out of the base
- ☐ Into the base and out of the emitter
- ☐ Into the base and out of the collector

13. Calculate the base voltage.

_____

_____

14. Calculate the base current.

15. Calculate the collector current.

16. Calculate the collector voltage.

Questions 17 to 26 refer to the circuit in Figure 3

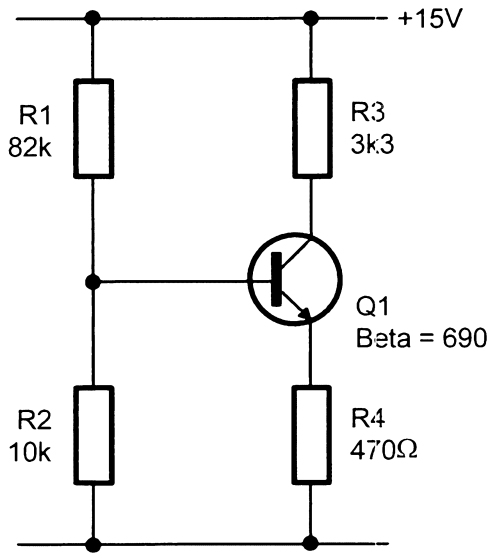

Figure 3

17. What biasing method does the circuit use?

18. Calculate the base voltage.

19. Calculate the emitter voltage.

20. Calculate the collector current.

21. Calculate the collector voltage.

22. Calculate the collector-emitter voltage.

23. Calculate the collector-base voltage.

24. What is the function of *R3*?

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25. What is the function of *R4*?

26. What is the function of resistors *R1* and *R2*?

Questions 27 to 32 refer to the circuit in Figure 4

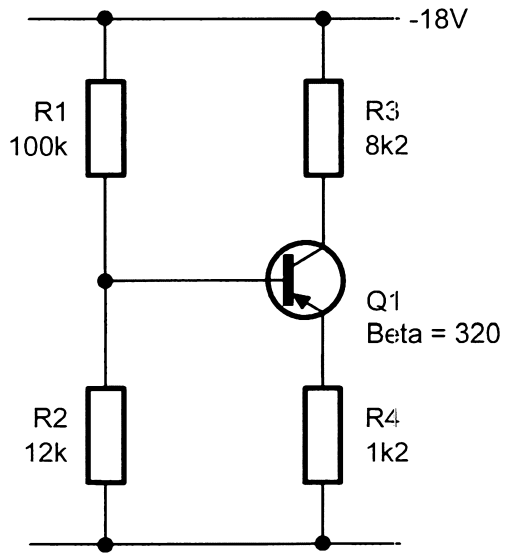

Figure 4

27. Calculate the base voltage.

28. Calculate the emitter voltage.

29. Calculate the collector current.

30. Calculate the collector voltage.

31. Calculate the collector-emitter voltage.

32. Calculate the collector-base voltage.

33. Determine the value of *R2* in Figure 4 if the potential difference across *R3* is 3.3V.

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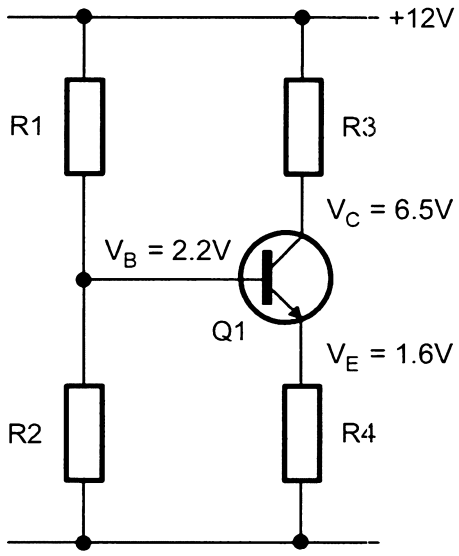

Figure 5

34. Figure 6 above shows a voltage divider biased NPN BJT circuit and its normal quiescent DC voltages. Table 1 below lists the voltages measured around the circuit for six faults. Use this information to determine the likely cause of each fault.

Table 1

V_B	V_E	V_C	Cause
0V	0V	12V	
1.7V	1.7V	12V	
2.2V	1.6V	12V	
4V	3.6V	4.4V	
2.2V	1.6V	4.4V	
2.2V	2.4V	2.4V	

Section 3 BJT amplifier configurations

Purpose To develop your knowledge and skills to help you recognise amplifier faults by measuring the output signal from a BJT amplifier and comparing it to the predicted output for its configuration and for a known input.

Objectives At the end of the lesson you should be able to:

- Identify the three BJT amplifier configurations
- Identify the input and output terminals of each configuration
- Describe the effects on the quiescent voltages and currents around the BJT configurations when an input signal is connected
- State the signal input-output phase relationship for each configuration
- List the main characteristics and applications of each configuration
- State the two factors that determine the maximum peak-to-peak output voltage of a BJT amplifier
- Calculate the maximum peak-to-peak output voltage of a BJT amplifier
- Measure the gain, phase relationship and maximum peak-to-peak output voltage of a common emitter and common collector BJT amplifier

Introduction

The previous chapters have introduced you to transistor biasing - that is, the setting up the transistor's DC conditions necessary to make it work as an amplifier. This chapter deals with how these circuits work as small signal voltage amplifiers.

Amplifier configurations

As you know, the BJT is a current amplifying device. The BJT's input is the base current and its output is the collector current. However, applying an AC signal voltage to the point in a BJT biasing circuit produces other AC voltages in the circuit that are a copy of the input signal and often larger. In other words, the circuits can be made to amplify signal voltages.

There are three methods of achieving this and they're known as the *BJT amplifier configurations*. They are:

- The common emitter configuration
- The common collector configuration
- The common base configuration

The input and output connections for each are shown using the simplified NPN BJT circuits in Figures 1a to 1c below.

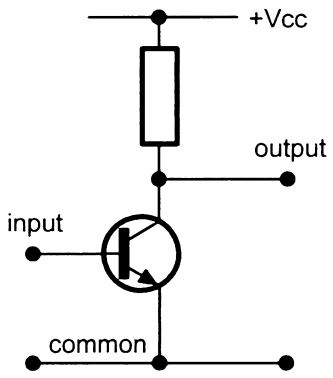

Figure 1a *Common emitter*

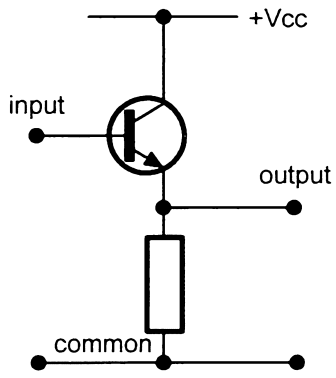

Figure 1b *Common collector*

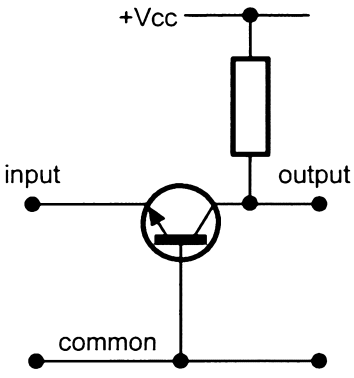

Figure 1c *Common base*

Notice that in each case, the 0V reference rail is part of both the input and output connections. In other words the 0V reference is common to both the input and output circuit which explains why it's called "common". Up to relatively recently, the common line was always connected to earth via the plug's earth pin. However, an electrical connection from common to earth is now unnecessary for most domestic electronics equipment where the double-insulation method for preventing electric shock is used. This means that the common line inside electronics equipment is seldom earthed these days.

The following notes explain the operation of the three configurations using base bias and/or voltage divider bias circuits.

Common emitter BJT amplifiers

Figure 2 below shows a base biased common emitter NPN BJT amplifier.

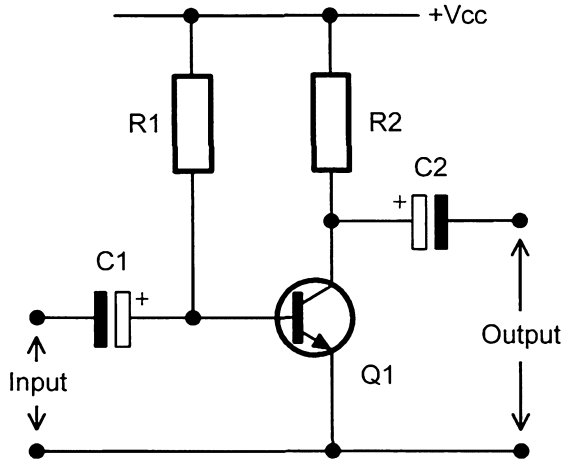

Figure 2 *A base biased common emitter NPN BJT amplifier*

How the circuit works as a voltage amplifier

As you know, the DC voltage on the base of the BJT in a base bias circuit is 0.6V. And, the voltage on the collector (with respect to common) is some bigger positive voltage but less than the supply voltage. Let's say in this example, the collector voltage is 5V.

These voltages are known as the *quiescent* voltages ("quiescent" means quiet or "steady-state") and they're shown as graphs in Figure 3.

Without an input signal, these voltages stay this way for as long as power is connected to the circuit.

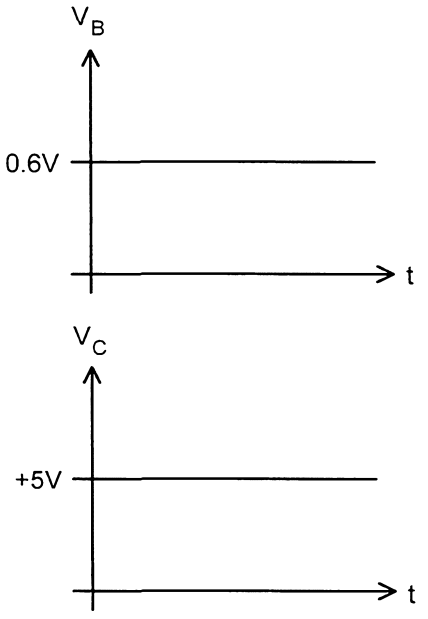

Figure 3

When an AC signal is connected to the amplifier's input, it is superimposed onto the quiescent base voltage as shown in Figure 4. This causes the BJT's base voltage to go up and down in sympathy with the input signal (so the base voltage is no-longer quiescent).

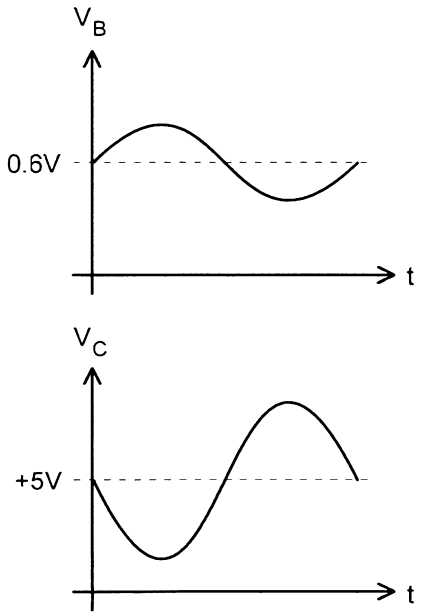

Figure 4

As the BJT's emitter is directly connected to common, the emitter voltage is held at 0V. So, when the input signal's voltage increases towards the positive peak, the BJT's base-emitter voltage (V_{BE}) increases also. This causes the base-emitter junction to become more forward biased causing more collector current to flow. As the collector current increases, so does the potential difference across the collector resistor which, in turn, reduces the voltage at the collector (with respect to common).

Then, as the input signal's polarity reverses and heads towards the negative peak, the BJT's base-emitter voltage decreases. This causes the base-emitter junction to become less forward biased so less collector current flows. As the collector current decreases, so does the potential difference across the collector resistor which, in turn, increases the voltage at the collector (with respect to common).

The result is a varying DC voltage on the collector that is a phase-inverted copy of the input signal and may be up to 300 times larger.

Figure 5 below shows base biased common emitter amplifiers with PNP BJTs using both positive and negative supply voltages.

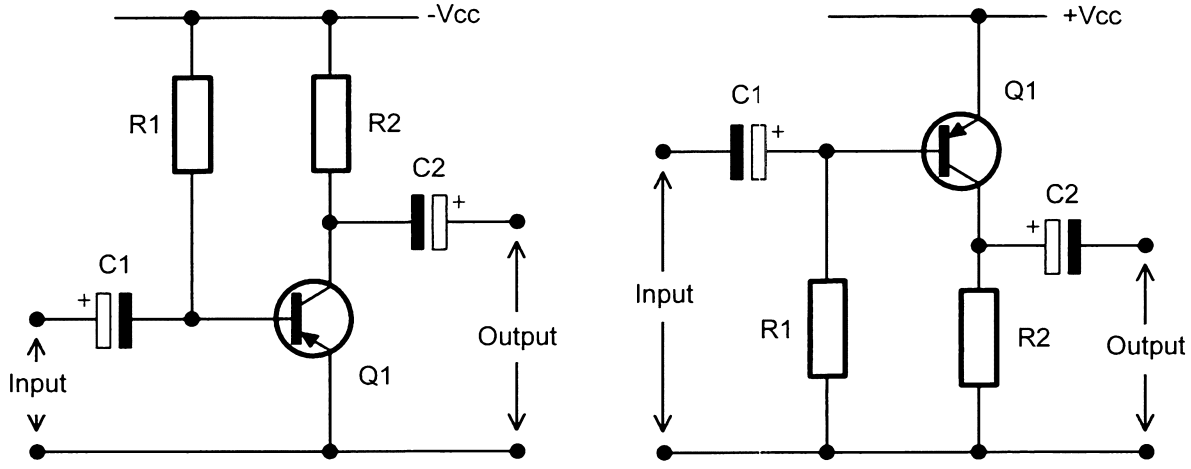

Figure 5 *Base biased common emitter PNP BJT amplifiers with: left) a $-V_{CC}$; and right) a $+V_{CC}$*

Figure 6 below shows a voltage divider biased common emitter NPN BJT amplifier. Importantly, the circuit is still a common emitter configuration even though the BJT's emitter isn't directly connected to common.

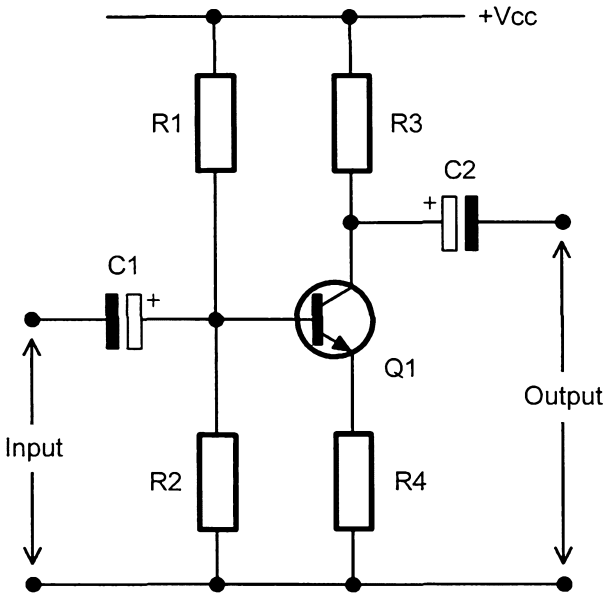

Figure 6 *Voltage divider biased common emitter NPN BJT amplifier*

How the circuit works as a voltage amplifier

As you know, the quiescent DC voltage on the base of a BJT in a voltage divider bias circuit is some voltage less than the supply. Let's say in this example that it's 1.6V. As you also know, the quiescent emitter voltage of the voltage divider bias circuit is 0.6V lower than the base voltage (for an NPN BJT). So, if the base voltage is 1.6V then the emitter voltage is 1V.

The size of emitter current is determined by the emitter voltage and the value of the emitter resistor ($I_E = \frac{V_E}{R_E}$) which in turn sets the collector current. The collector current develops a potential difference across the collector resistor making the collector voltage less than the supply voltage (with respect to common). For the purposes of this explanation, let's say that the collector voltage is 5V.

The quiescent base and collector voltages are shown in Figure 7.

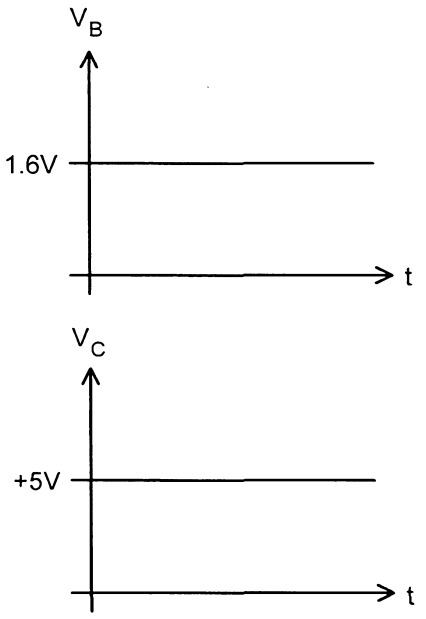

Figure 7

When an AC signal is connected to the amplifier's input, it is superimposed onto the quiescent base voltage (see Figure 8). This causes the BJT's base voltage to go up and down in sympathy with the input signal.

As the input signal increases towards the positive peak, the emitter voltage (V_E) increases also because it stays 0.6V lower than the base voltage.

This increase in emitter voltage causes an increase in collector current which increases the potential difference across the collector resistor and decreases the voltage at the collector (with respect to common).

Then, as the input signal reverses polarity and heads towards the negative peak, the emitter voltage decreases also. So the collector current goes down decreasing the potential difference across the collector resistor and increasing the voltage at the collector (with respect to common).

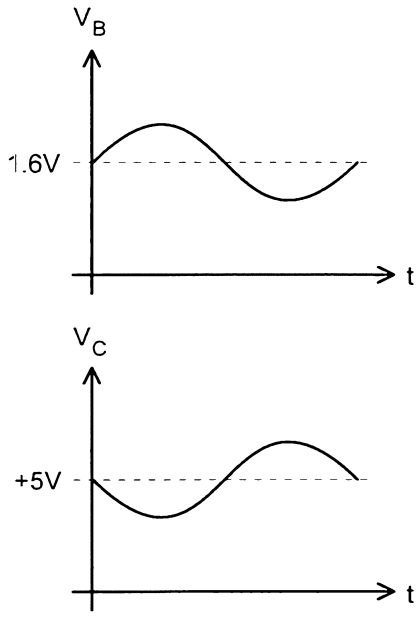

Figure 8

The result is a varying DC voltage on the collector that is a phase-inverted copy of the input signal that is between 3 to 300 times larger.

Figure 9 below shows two voltage divider biased common emitter amplifiers with PNP BJTs using both negative and positive supply voltages.

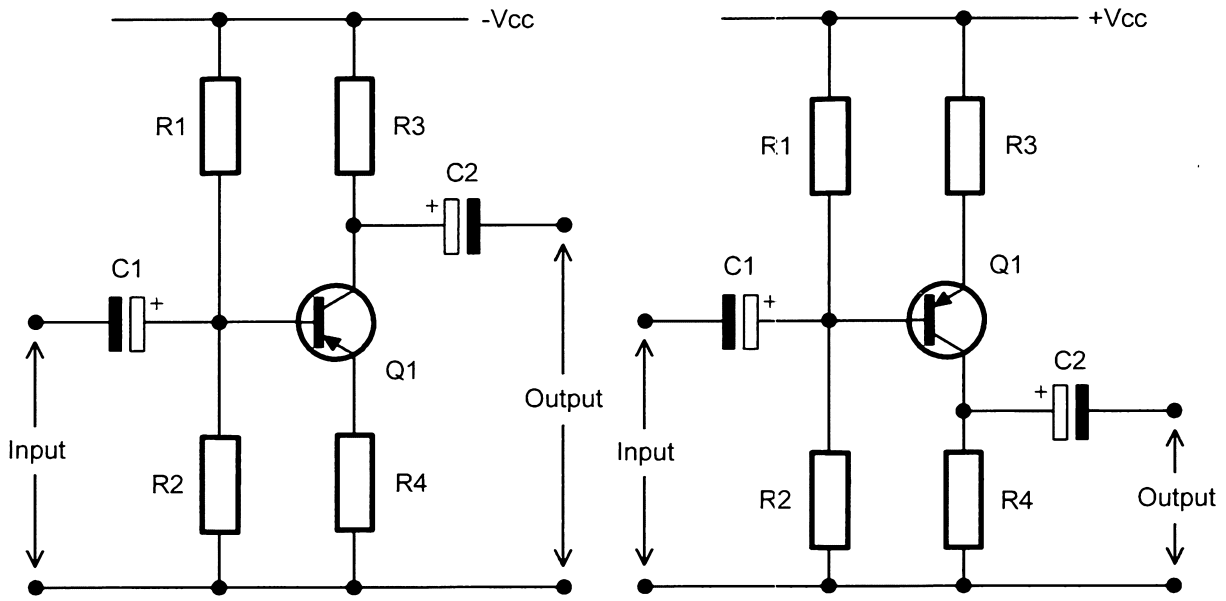

Figure 9 *Voltage divider biased common emitter PNP BJT amplifiers: (left) with -V_{CC}; (right) with +V_{CC}*

Common emitter amplifier characteristics
The characteristics and applications of common emitter amplifiers are:

- The input is connected to the base.
- The output is taken from the collector.
- The output signal is phase inverted compared to the input signal.
- It has a low to high voltage gain (typically 3 to 300 depending on whether the emitter resistor has been by-passed).
- It has a medium to high input resistance (typically 3kΩ to 30kΩ).
- It has a medium to high output resistance (typically 1kΩ to 50kΩ).
- It is mainly used to amplify small voltage signals such as those from a microphone, electric guitar, CD player and radio transmitter or receiver.

Common collector BJT amplifiers

Figure 10 below shows a voltage divider biased common collector NPN BJT amplifier. Notice that the circuit doesn't have a collector resistor. This is because the output is taken from the emitter so the collector resistor is unnecessary.

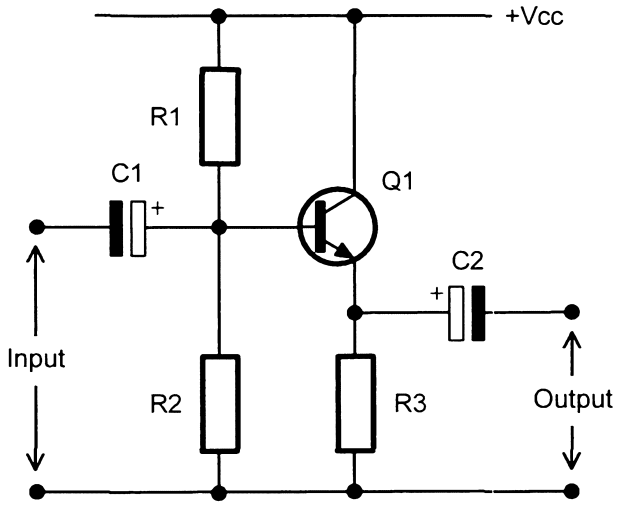

Figure 10 *A voltage divider biased common collector NPN BJT amplifier*

How the circuit works as a voltage amplifier

As you know, the quiescent DC voltage on the base of the BJT in a voltage divider bias circuit is some voltage less than the supply. Let's say in this example that it's 5.6V. As you also know, the quiescent emitter voltage of the voltage divider bias circuit is 0.6V lower than the base voltage (for an NPN BJT). So, if the base voltage is 5.6V the emitter voltage is 5V.

These quiescent voltages are shown in Figure 11. And, without an input signal, these voltages will stay this way for as long as power is connected to the circuit.

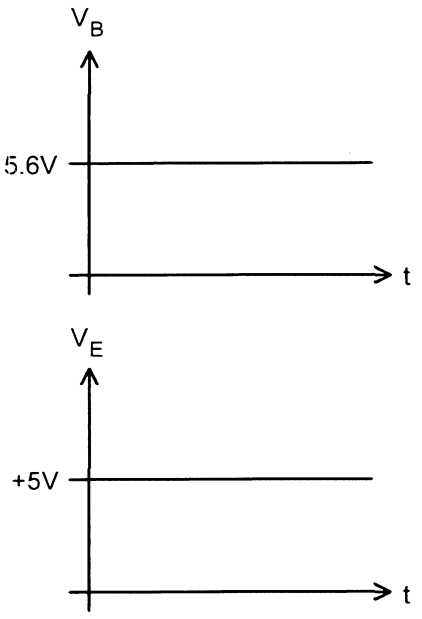

Figure 11

When an AC signal is connected to the amplifier's input, it is superimposed onto the quiescent base voltage (see Figure 12). This causes the BJT's base voltage to go up and down in sympathy with the input signal.

As the input signal increases towards the positive peak, the emitter voltage increases also because it wants to stay 0.6V lower than the base voltage.

Then, as the input signal reverses polarity and heads towards the negative peak, the emitter voltage decreases so that it stays 0.6V lower than the base voltage.

The result is a varying DC voltage on the emitter that is an in-phase copy of the input signal and slightly smaller than it.

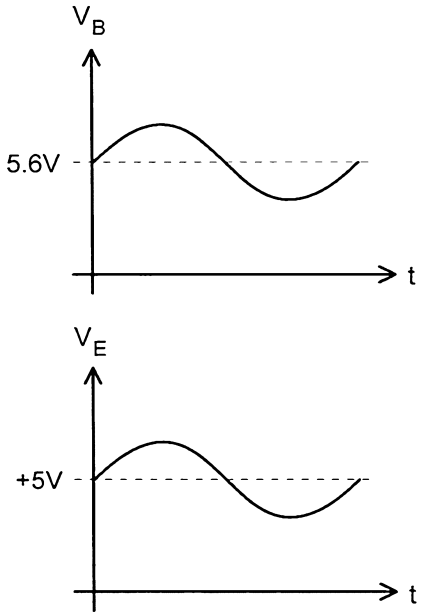

Figure 12

Common collector amplifier characteristics

The characteristics and applications of common collector amplifiers are:

- The input is connected to the base.
- The output is taken from the emitter.
- The input and output signals are in-phase.
- The voltage gain is slightly less than one.
- The common collector is also often called an *emitter follower* because the output voltage follows (is the same as) the input voltage.
- It has a medium to high input resistance (typically 10kΩ to 100kΩ).
- It has a low output resistance (typically tens of ohms).
- It is mainly used as a buffer or isolation stage. Also used as a driver for loudspeakers because of its power gain. Also used as an *impedance matching* stage because it matches high to low impedance circuits.

Common base BJT amplifiers

Figure 13 below shows a voltage divider biased common base NPN BJT amplifier.

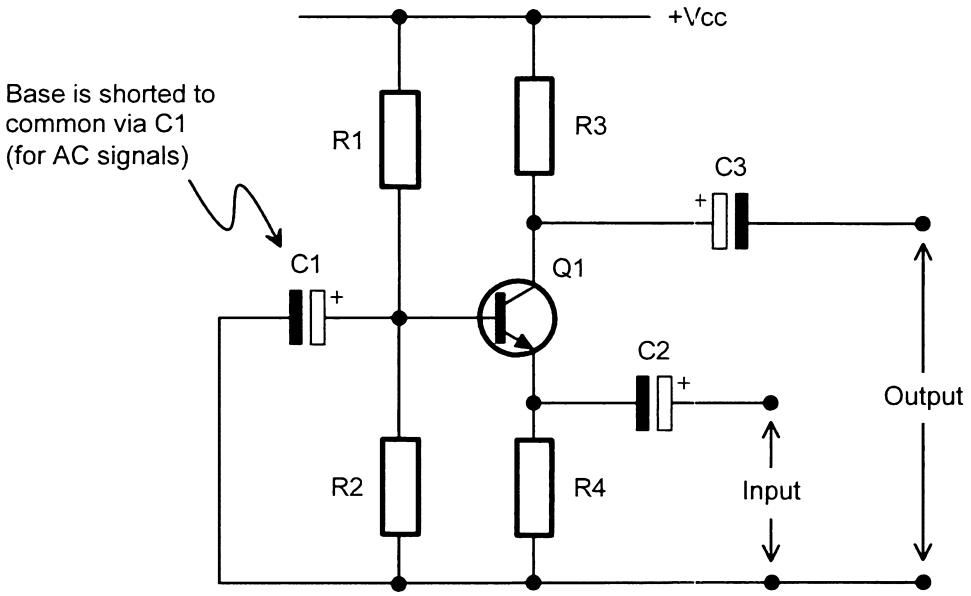

Figure 13 *A voltage divider biased common base NPN BJT amplifier*

How the circuit works as a voltage amplifier

As you know, the quiescent DC voltage on the base of the BJT in a voltage divider bias circuit is some voltage less than the supply. Let's say in this example that it's 1.6V. As you also know, the quiescent emitter voltage of the voltage divider bias circuit is 0.6V lower than the base voltage (for an NPN BJT). So, if the base voltage is 1.6V the emitter voltage is 1V.

The size of emitter current is determined by the emitter voltage and the value of the emitter resistor ($I_E = \frac{V_E}{R_E}$) which in turn sets the collector current. The collector current develops a potential difference across the collector resistor which makes the collector voltage less than the supply voltage (with respect to common). For the purposes of this explanation, let's say that the collector voltage is 5V. These *quiescent* emitter and collector voltages are shown in Figure 14.

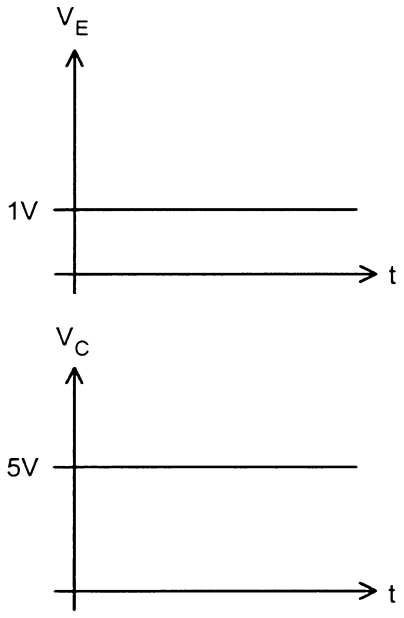

Figure 14

When an AC signal is connected to the amplifier's input, it is superimposed onto the quiescent emitter voltage (see Figure 15). This causes the BJT's emitter voltage to go up and down in sympathy with the input signal.

As the input signal increases towards the positive peak, the emitter voltage increases also. This increase in emitter voltage causes a decrease in the BJT's base-emitter voltage because the base voltage is held constant by the voltage divider. A decrease in base-emitter voltage causes a decrease in collector current which causes a decrease in potential difference across the collector resistor and so the voltage at the collector increases (with respect to common).

Then, as the input signal reverses polarity and heads towards the negative peak, the emitter voltage decreases also. So the base-emitter voltage and collector current go up, increasing the potential difference across the collector resistor and decreasing the voltage at the collector (with respect to common).

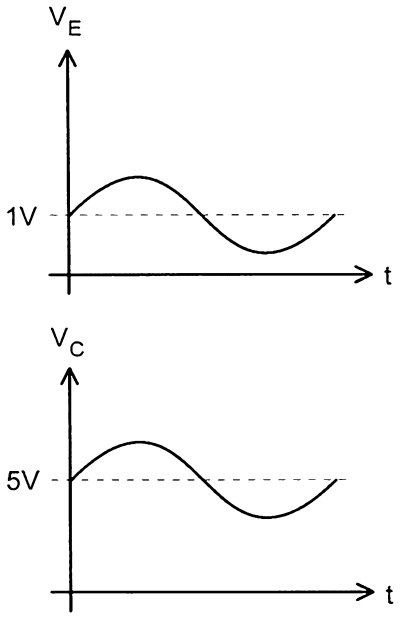

Figure 15

The result is a varying DC voltage on the collector that is an in-phase copy of the input signal and up to 300 times larger.

Common base amplifier characteristics

The characteristics and applications of common base amplifiers are:

- The input is connected to the emitter.
- The output is taken from the collector.
- The input and output signals are in-phase.
- It has a high voltage gain (similar to common emitter).
- It has a wider bandwidth than the other two configurations (>10MHz).
- It has a very low input resistance (typically around 30Ω).
- It has a medium to high output resistance (similar to common emitter).
- It is mainly used to amplify small signal voltages in high frequency (radio) circuits because its gain remains high at these frequencies, unlike the common emitter's gain which starts to fall.

Comparisons between the three configurations

Table 1 shows a comparison of the three amplifier configurations.

Table 1

Parameter	Common emitter	Common collector	Common base
Voltage gain	Low to high	**Slightly less than one**	High
Input resistance	Medium to high	Medium to high	**Very low**
Output resistance	Medium to high	**Low**	Medium to high
Phase relationship	**Inverted**	In-phase	In-phase
Main use	Signal amplifier	Buffer	RF comms

Factors affecting the maximum peak-to-peak output

Recall from your work with op amps that if you overdrive an amplifier (that is, you make the input signal too big) the output signal is clipped. This is also true of transistor amplifiers.

There are two factors that directly affect the maximum peak-to-peak output voltage of unloaded BJT amplifiers before clipping. They are:

- The size of the supply voltage
- The quiescent DC voltage on the transistor's terminal that the output is taken from (either the collector or the emitter depending on the configuration)

These are shown on the circuits of a common emitter and common collector BJT amplifier in Figure 16 below.

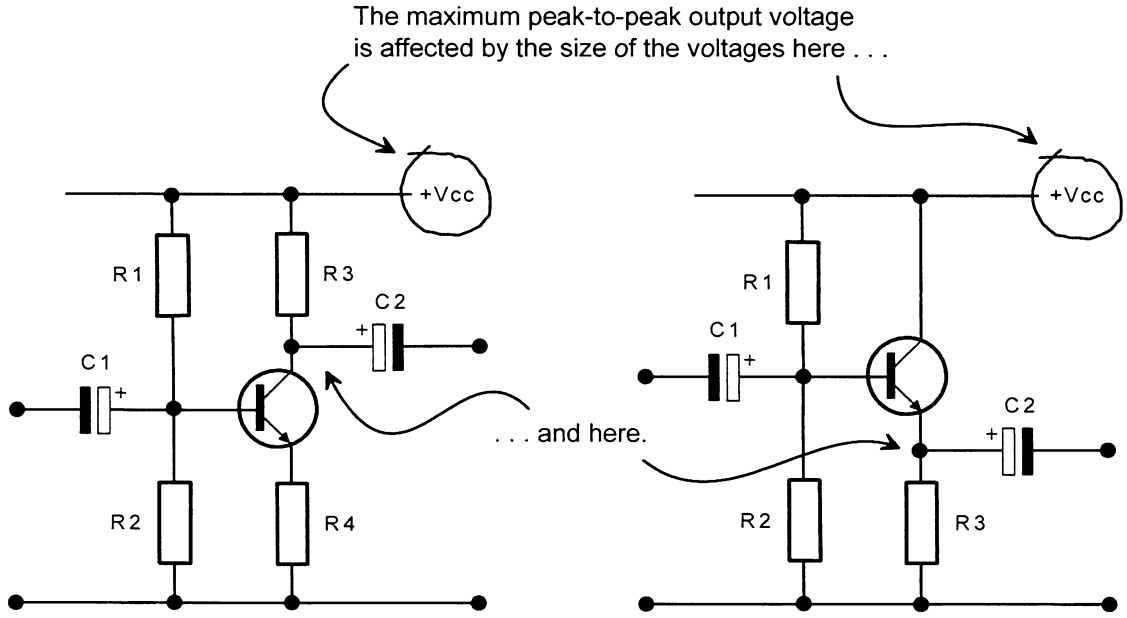

Figure 16 *The maximum peak-to-peak output voltage before clipping is affected by the supply voltage and the quiescent DC voltage on the collector (of the common emitter BJT amplifier) or the emitter (of the common collector BJT amplifier)*

The fact that the supply voltage affects the maximum peak-to-peak output voltage before clipping should not be a surprise to you following your earlier studies of op amps. Without a transformer or an additional power source, it's impossible for the voltage on the BJT's output terminal to exceed zero volts or the supply voltage. If they attempt to, the signal gets chopped-off producing a classic case of clipping as shown in Figure 17 below.

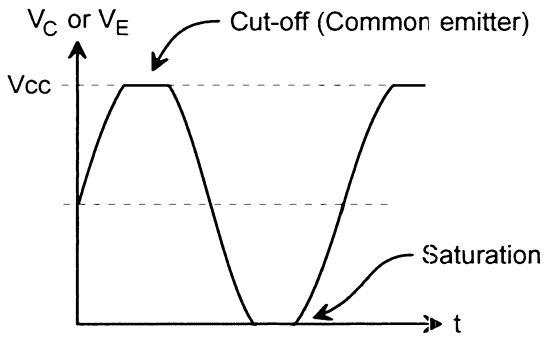

Figure 17 *The classic case of clipping that results when the BJT's output terminal attempts to exceed 0V or the supply voltage*

To understand why the quiescent DC voltage on the BJT's output terminal affects the maximum peak-to-peak output voltage before clipping, you must fully appreciate that the DC output voltage forms the output signal's axis of symmetry (or its centre line). This is emphasised in Figure 18 below.

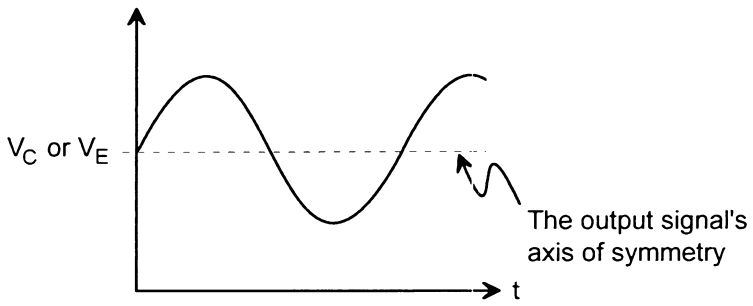

Figure 18 *The voltage on the BJT's output terminal forms the axis of symmetry for the output signal*

The position of the quiescent DC voltage on the output terminal relative to zero volts and the supply voltage affects how far the signal can travel before it reaches zero volts or the supply voltage. This is demonstrated in Figure 19 below using a variety of collector/emitter voltages.

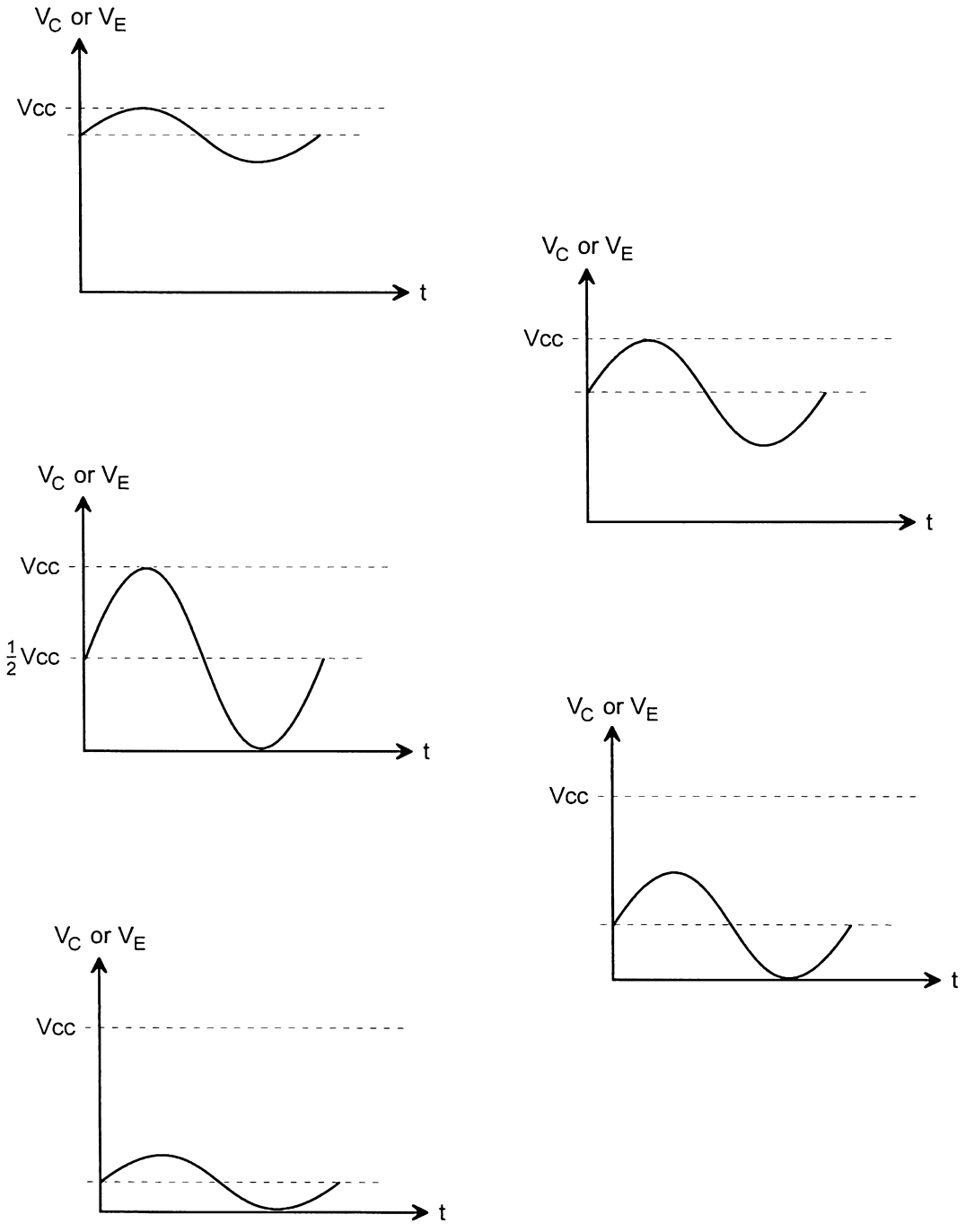

Figure 19

Figure 19 clearly demonstrates that the maximum peak-to-peak output voltage without clipping is achieved when the BJT's output terminal voltage is about half the supply voltage.

If the quiescent DC voltage is closer to the supply voltage, there's less room for the output signal's positive half cycle than there is for the negative half cycle. So, as the input signal gets too big, clipping first appears on the top of the output signal as shown in Figure 20 below.

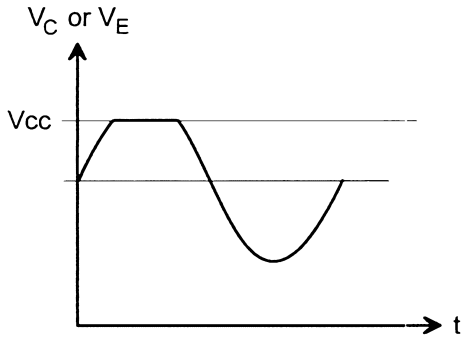

Figure 20

If the quiescent DC voltage is closer to zero volts, there's less room for the output signal's negative half cycle than there is for its positive half cycle. So, as the input signal gets too big, clipping first appears on the bottom of the output signal as shown in Figure 21 below.

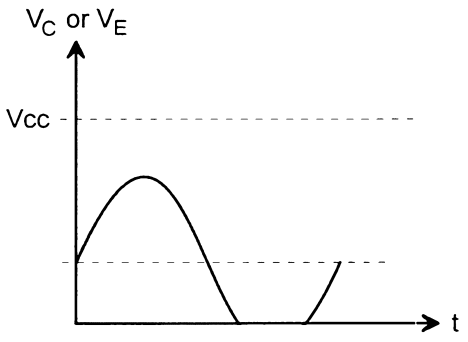

Figure 21

Calculating the maximum peak-to-peak output and input voltages

To calculate the maximum peak-to-peak output voltage for an unloaded BJT amplifier circuit you must first compare the quiescent DC voltage on the transistor's output terminal to the supply voltage. If the voltage on the output lead is less than half of the supply voltage then the maximum peak-to-peak output voltage is found using the equation:

Common emitter: $Vout_{(max)} = V_C \times 2$

Common collector: $Vout_{(max)} = V_E \times 2$

If the voltage on the output lead is more than half of the supply voltage then the maximum peak-to-peak output voltage is found using the equation:

Common emitter: $Vout_{(max)} = (V_{CC} - V_C) \times 2$

Common collector: $Vout_{(max)} = (V_{CC} - V_E) \times 2$

Once the maximum peak-to-peak output voltage before clipping is known, the maximum input voltage can be found using the equation:

$$Vin_{(max)} = \frac{Vout_{(max)}}{Av}$$

Note: This discussion on maximum peak-to-peak output voltage and these equations assume an amplifier that is not loaded or only relatively lightly loaded. The analysis becomes more complicated for more heavily loaded amplifiers and is not discussed here.

Practise calculating the maximum output and inputs voltages for BJT amplifiers by trying the following examples.

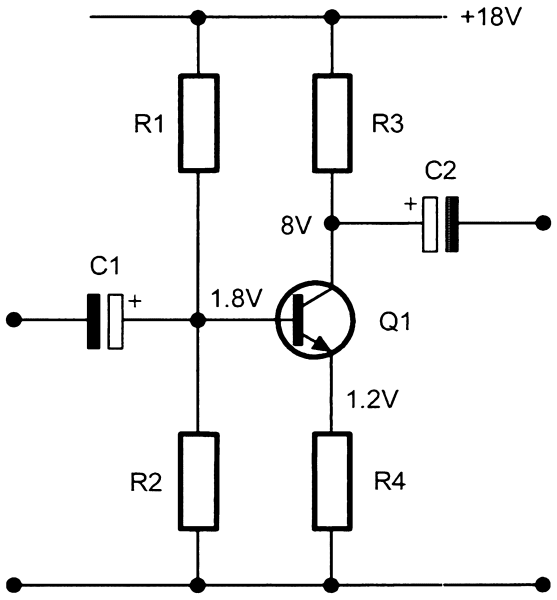

Figure 22

1. Determine the maximum peak-to-peak output voltage before clipping for the circuit in Figure 22.

2. On which half of the output signal will the clipping appear first if the amplifier is overdriven?

3. Calculate the maximum input voltage of the amplifier if it has a voltage gain of 170.

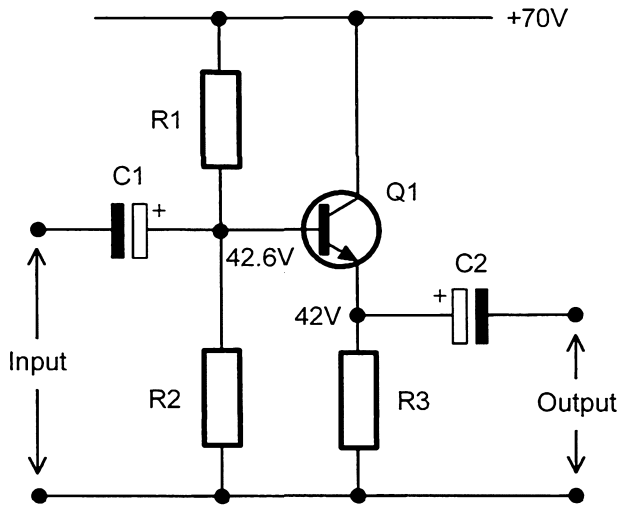

Figure 23

4. Determine the maximum peak-to-peak output voltage before clipping for the circuit in Figure 23.

5. On which half of the output signal will the clipping appear first?

Connecting inputs signals to transistor amplifiers

Not surprisingly, in most cases, there's a right way and a wrong way to connect a signal source to the input of a transistor amplifier. If they're connected to each other the wrong way then, at best, the amplifier will malfunction. At its worst, the mistake can result in damage to the signal source.

The key to making your input connections correctly is to remember that the inputs and outputs to most transistor amplifiers and the devices that connect to them are *unbalanced.* That is, the signal is present at only one of the two terminals. The other terminal is the circuit's common (which is zero volts). This is shown in Figure 24 below.

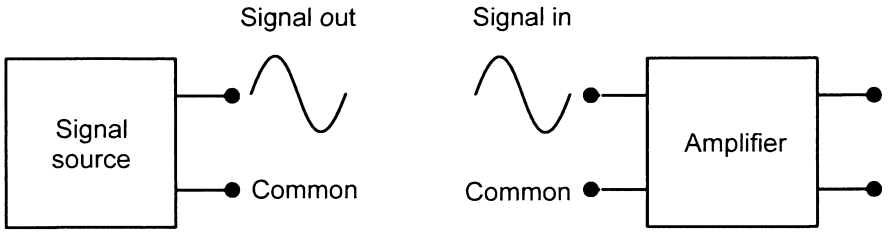

Figure 24 *The unbalanced output of a signal source and the unbalanced input and output of the amplifier*

The correct way to connect the signal source to the amplifier is to connect the terminal from which the signal comes out of the source to the terminal that the signal should go into on the amplifier. The two common terminals are connected together. This is shown in Figure 25 below.

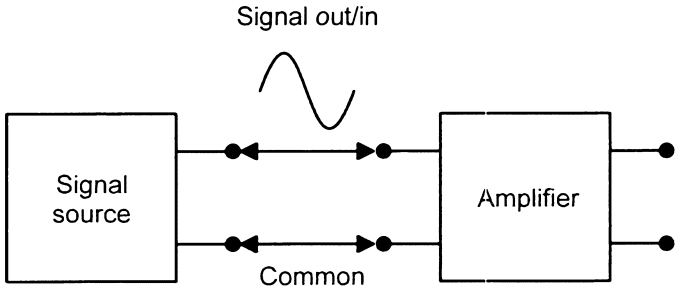

Figure 25 *The unbalanced output of a signal source correctly connected to the unbalanced input of the amplifier*

This may seem obvious but it is common for people new to working with discrete transistor amplifier circuits to connect the source to the amplifier with the terminals connected in the wrong polarity (as shown in Figure 26 below).

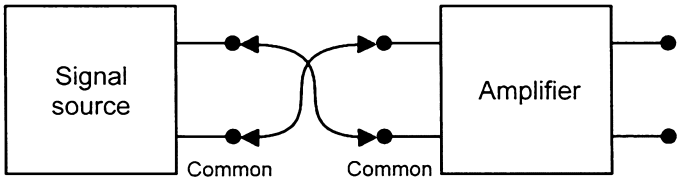

Figure 26 *The unbalanced output of a signal source incorrectly connected to the unbalanced input of the amplifier*

When this happens the terminal for the input signal to the amplifier is connected to the common of the signal source and so the amplifier doesn't have an input signal. This makes the amplifier appear as though it's not working.

Worse than this, the output terminal of the signal source is connected to the common of the amplifier which pulls down the signal source's output voltage and can damage its output circuitry.

So, when you're working on transistor amplifiers in the practical exercises, always make sure that the black alligator-clip on the lead from the signal source (and the CRO too) is connected to the amplifier's common line. This will ensure that you're always connecting your input signal to the transistor amplifier in the correct polarity.

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Student notes

Skill practice 3

Practise measuring AC voltages in BJT amplifiers using an oscilloscope

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 1¼ hours to complete this exercise.

Equipment

- Emona Trainer
- DMM
- BC549 transistor
- two 120kΩ ¼W resistors
- 15kΩ ¼W resistor
- 2k2Ω ¼W resistor
- 5k6Ω ¼W resistor
- 270Ω ¼W resistor
- two 1µF capacitors (electrolytic)
- three BNC to alligator-clip leads
- banana leads
- hook-up wire
- wire strippers

Remember:

Follow TAFE NSW WHS guidance at all times!

Work tasks

1. Read your WHS responsibilities at the top of the form below. Then conduct a WHS risk assessment and record your findings in the space provided.

Responsibilities of students under the Model WHS Act: s28

- Take reasonable care for your own health and safety by working safely at all times
- Take reasonable care to ensure that your acts or omissions don't put the health and safety of others at risk
- Follow all TAFE NSW WHS guidance and comply with all reasonable instructions from TAFE NSW staff to assist them in complying with the TAFE NSW WHS requirements
- In addition to the above, you must:
  - use and maintain machinery, tools and all other equipment properly and safely
  - ensure that your work area is free of hazards
  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

Risks involved in this activity include:	**Control measures:**
Trip hazards (eg students bags) Objects dropped on feet (while equipment is taken to and from workbenches).	Move bags and other objects from walkways Plan lifting of equipment
Others: _____	Other: _____
_____	_____
_____	_____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

3. Turn off the Emona Trainer then wire the circuit of Figure 1.

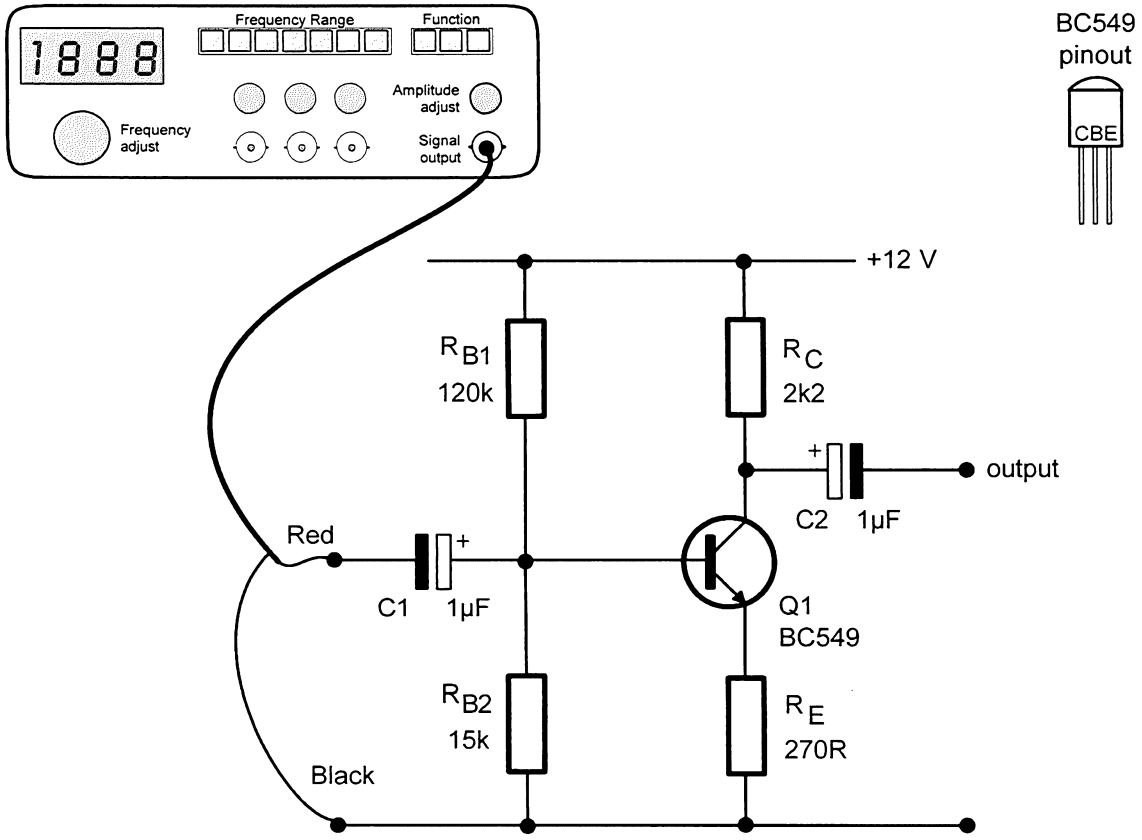

Figure 1

4. Switch on the Emona Trainer but **don't** switch on the signal generator.

5. Measure the base-emitter voltage (V_{BE}) using the DMM.

   Self-check: If the base-emitter voltage (V_{BE}) is between 0.55V and 0.7V then your circuit is probably working so go to Step 6. If V_{BE} is not within this range then there is probably something wrong with the circuit. Check your wiring but if you still can't get the circuit working, call the teacher.

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6. Calculate the theoretical quiescent DC voltages at each terminal of the transistor. Record your calculations in Table 1 below.

7. Measure and record these voltages with a DMM.

Table 1	Theoretical (Step 6)	Measured (Step 7)
Base voltage (V_B)		
Emitter voltage (V_E)		
Collector voltage (V_C)		

The teacher needs to check your work at this point...

8. Turn on the signal generator.

9. Connect the CRO's channel 1 input to the amplifier's input.

10. Set the signal generator to produce a 1kHz sinewave at 500mVp-p.

11. Connect the CRO's channel 2 input to the amplifier's output.

12. Measure the output voltage. Record your measurement in Table 2 below.

13. Calculate and record the gain using your measured values of input and output voltage.

14. Observe and record the phase relationship between the input and output signals.

Table 2

Input voltage	Output voltage	Measured gain	Phase relationship
500mVp-p			

Question 1
What amplifier configuration is the circuit in Figure 1?

Question 2
What is the typical range of gains for this configuration (refer to your notes for this information)? Does the gain of your circuit fall within this range?

Question 3
What is the theoretical input-output phase relationship for this configuration (refer to your notes for this information)? Is the phase relationship of your circuit correct?

The teacher needs to check your work at this point...

15. Determine the circuit's theoretical maximum peak-to-peak output voltage using your measured value of collector voltage (V_C). Record the value in Table 3 below.

16. Find the circuit's maximum peak-to-peak output voltage by increasing the amplitude of the input signal until the output signal is just about to clip. Record your measurement in Table 3.

Table 3	Theoretical	Measured
Maximum peak-to-peak output voltage		

Question 4
Calculate the maximum peak-to-peak input voltage allowable before the signal source starts to overdrive the amplifier.

Question 5
Which two circuit voltages determine the amplifier's maximum peak-to-peak output voltage?

The teacher needs to check your work at this point...

17. Turn off both the Emona Trainer and signal generator.

18. Wire the circuit of Figure 2 below.

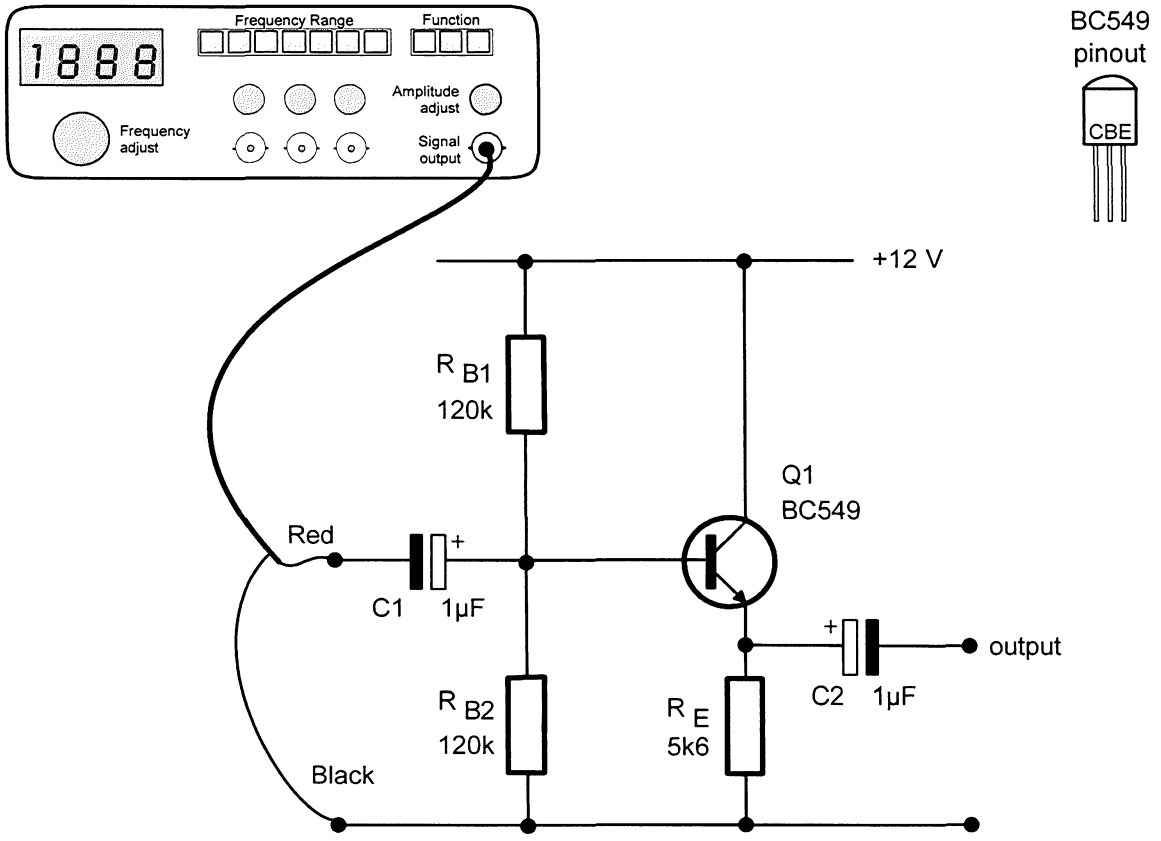

Figure 2

19. Switch on the Emona Trainer but **don't** switch on the signal generator.

20. Measure the base-emitter voltage (V_{BE}) using the DMM.

    Self-check: If the base-emitter voltage (V_{BE}) is between 0.55V and 0.7V then your circuit is probably working so go to Step 21. If V_{BE} is not within this range then there is probably something wrong with the circuit. Check your wiring but if you still can't get the circuit working, call the teacher.

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21. Calculate the theoretical quiescent DC voltages at each terminal of the transistor. Record your calculations in Table 4 below.

22. Measure and record these voltages with a DMM.

Table 4	Theoretical	Measured
Base voltage (V_B)		
Emitter voltage (V_E)		
Collector voltage (V_C)		

The teacher needs to check your work at this point...

23. Turn on the signal generator.

24. Connect the CRO's channel 1 input to the amplifier's input.

25. Set the signal generator to produce a 1kHz sinewave at 500mVp-p.

26. Connect the CRO's channel 2 input to the amplifier's output.

27. Measure the output voltage. Record your measurement in Table 5 below.

28. Calculate and record the gain using your measured values of input and output voltage.

29. Observe and record the phase relationship between the input and output signals.

Table 5

Input voltage	Output voltage	Measured gain	Phase relationship
500mVp-p			

Question 6
What amplifier configuration is the circuit in Figure 2?

Question 7
What is the typical gain for this configuration (refer to your notes for this information)? Is the gain of your circuit correct?

Question 8
What is the theoretical input-output phase relationship for this configuration (refer to your notes for this information)? Is the phase relationship of your circuit correct?

The teacher needs to check your work at this point...

30. Determine the circuit's theoretical maximum peak-to-peak output voltage using your measured value of emitter voltage (V_E). Record the value in Table 6 below

31. Find the circuit's maximum peak-to-peak output voltage by increasing the amplitude of the input signal until the output signal is just about to clip. Record your measurement in Table 6.

Table 6	Theoretical	Measured
Maximum peak-to-peak output voltage		

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Question 9
Calculate the maximum peak-to-peak input voltage allowable before the signal source starts to overdrive the amplifier?

Question 10
Which two circuit voltages determine the amplifier's maximum peak-to-peak output voltage?

The teacher needs to check your work at this point...

Review questions

Answer these questions to check your understanding of what you have learnt for this chapter. Doing this will also help to prepare you for the tests.

Questions 1 to 5 refer to the circuit in Figure 1

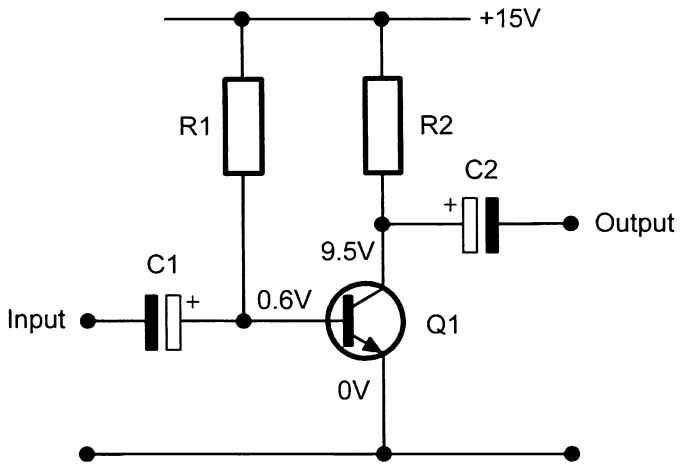

Figure 1

1. What amplifier configuration is the circuit?

   ☐ Common base
   ☐ Common collector
   ☐ Common emitter

2. What is a typical value for the gain of this configuration?

   ☐ Slightly less than 1
   ☐ Exactly 1
   ☐ Between slightly less than 1 and 200
   ☐ Between 3 and 300

3. Determine the circuit's maximum peak-to-peak output voltage.

   _____

   _____

4. Calculate the circuit's maximum peak-to-peak input voltage if its voltage gain is 120.

5. Which amplifier configuration has the lowest input resistance?

- ☐ Common base
- ☐ Common collector
- ☐ Common emitter

6. Which amplifier configuration has the highest input resistance?

- ☐ Common base
- ☐ Common collector
- ☐ Common emitter

7. Which amplifier configuration has an inverted output?

- ☐ Common base
- ☐ Common collector
- ☐ Common emitter

8. What are two other names for the common collector configuration?

9. Why is the common collector configuration also called an *emitter follower*?

10. Which amplifier configuration has a typical bandwidth beyond 10MHz?

- ☐ Common base
- ☐ Common collector
- ☐ Common emitter

11. Which of the three amplifier configurations is best suited to the following applications?

(a) A driver for a speaker _____

(b) A high-gain amplifier with medium to high input resistance _____

(c) To match an amplifier to a low resistance load _____

(d) An ultra high frequency amplifier _____

(e) To amplify the voltage signal from a microphone _____

(f) A current amplifier _____

Questions 12 to 15 refer to the circuit in Figure 2

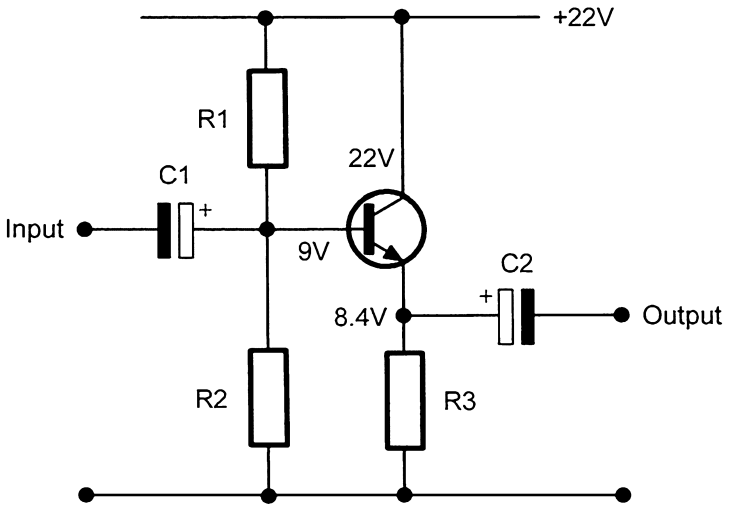

Figure 2

12. What amplifier configuration is the circuit?

☐ Common base
☐ Common collector
☐ Common emitter

13. What is a typical value for the gain of this configuration?

- ☐ Slightly less than 1
- ☐ Exactly 1
- ☐ Between slightly less than 1 and 200
- ☐ Between 3 and 300

14. Determine the circuit's maximum peak-to-peak output voltage.

_____

_____

_____

15. Calculate the circuit's maximum peak-to-peak input voltage.

_____

_____

Section 4 BJT amplifier AC parameters

Purpose To develop your knowledge of AC parameters of BJT amplifiers so that you can effectively test their operation and performance.

Objectives At the end of the lesson you should be able to:

- Calculate (using approximation equations) the voltage gain, input resistance and output resistance of the common emitter BJT amplifier configuration
- Calculate (using approximation equations) the voltage gain, input resistance and output resistance of the common collector BJT amplifier configuration
- Measure the unloaded and loaded voltage gain of the common emitter and common collector BJT amplifier configurations
- Measure the frequency response of BJT amplifiers

Introduction

The last chapter dealt with how BJT biasing circuits work as voltage amplifiers. This chapter continues the AC analysis of BJT circuits by looking at the BJT amplifier's AC parameters; specifically, the voltage gain, input resistance and output resistance of the common emitter and common collector configurations. (Note: You're not required to calculate the AC parameters for the common base configuration as its use is generally limited to high frequency applications and so you'll learn about it if you specialise in communications units in third year.)

Common emitter amplifier parameters

Consider the circuit in Figure 1 below. By now, you should recognise that it's a voltage divider biased, common emitter NPN BJT amplifier.

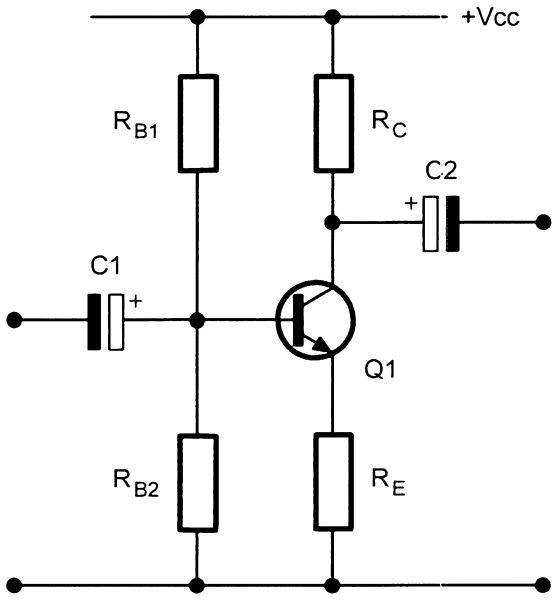

Figure 1 *A voltage divider biased, common emitter NPN BJT amplifier*

To determine the circuit's AC parameters it must be considered purely from the perspective an AC signal. When it is, the circuit looks very different. Recall that capacitors look like a short-circuit to AC signals (provided they're sufficiently large) so the capacitors in the circuit just look like wires. Recall also that there's a large filter capacitor connected across the output terminals of the power supply. So, from an AC perspective the V_{CC} and common are connected together.

The effect of these shorts around the AC circuit are shown in Figure 2 on the next page.

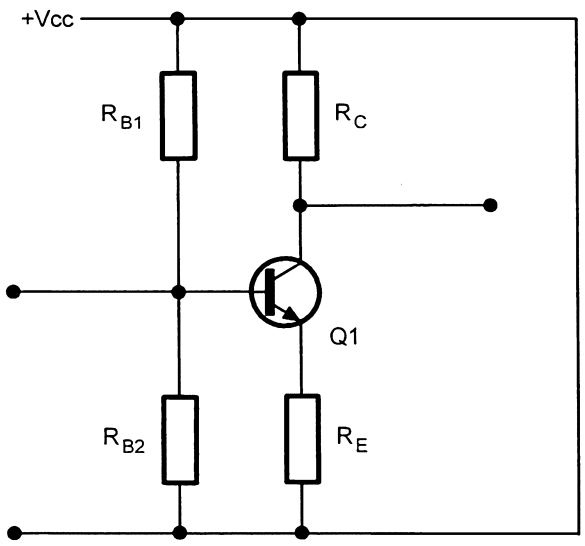

Figure 2 *A voltage divider biased, common emitter NPN BJT amplifier as seen by AC signals*

The circuit in Figure 2 can be simplified by redrawing it as shown in Figure 3 below.

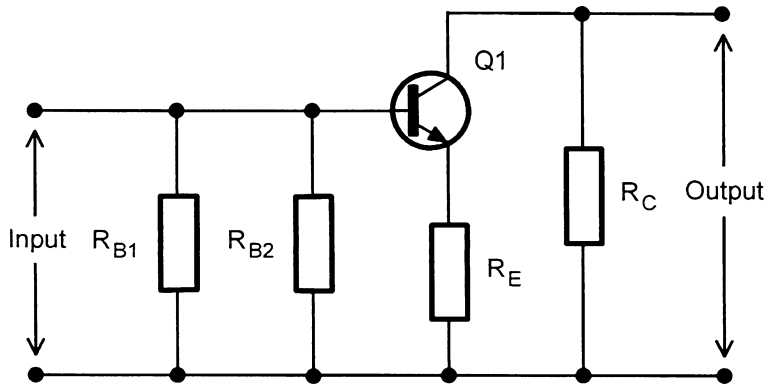

Figure 3 *The AC equivalent circuit in Figure 2 redrawn*

Drawn this way it can be seen that, from an AC perspective, R_{B1}, R_{B2} and the series combination of the transistor's base-emitter p-n junction and R_E are connected in parallel. Also, the resistor R_C appears to be connected to common.

To further the AC analysis, the BJT can be represented by the AC equivalent model shown in Figure 4 below.

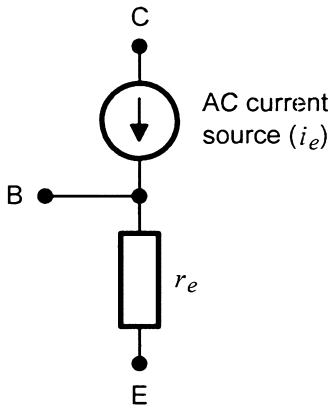

Figure 4 *The AC equivalent model of an NPN BJT*

When considered from a "black-box" perspective the BJT performs as though it has a current source inside it that generates the AC emitter current (which is really just the variation in the DC emitter current due to the input signal). The current source is in series with a resistor called the *dynamic emitter resistance* (r_e) and the base terminal is connected to the junction between them.

As its name implies, the dynamic emitter resistance is basically the forward biased base-emitter p-n junction's resistance due to changing currents through it. (Note: It's not necessary to consider r_e when performing the DC analysis of BJT circuits because, by definition, DC current doesn't change and so r_e is irrelevant.)

The size of r_e is usually relatively small and is set by the quiescent emitter current. The larger the emitter current, the smaller its resistance (naturally). Its value can be calculated with the equation shown below (provided the emitter current is less than 5mA):

$$r_e = \frac{26mV}{I_E}$$

Where:
r_e = dynamic emitter resistance
I_E = quiescent emitter current

When the NPN BJT in Figure 3 is substituted for its AC equivalent model we get the circuit in Figure 5 below. This is the complete AC equivalent circuit for the voltage divider biased common emitter NPN BJT amplifier in Figure 1.

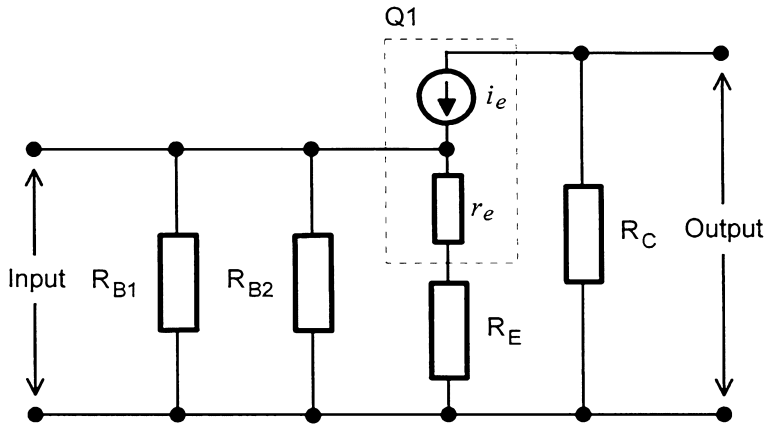

Figure 5 *The complete AC equivalent circuit for the circuit in Figure 1*

This circuit can now be used to help show how the equations for the AC parameters are derived. (**Note:** Test questions will not ask you to draw this circuit - It is developed here to show you how the following equations have been derived.)

Input resistance

If you consider the circuit in Figure 5, the resistance between the two input terminals appears to be the simple parallel combination of R_{B1}, R_{B2} and r_e in series with R_E. However, from the perspective of the input signal, the resistive effect of the series combination of r_e and R_E is magnified by the BJT's current gain (β). That being the case, the equation for calculating the input resistance is:

$$Rin = R_{B1} // R_{B2} // \beta \times (R_E + r_e)$$

To avoid using more maths to show why R_E+r_e must be multiplied by beta before calculating the input resistance, think of the issue this way. For a given input voltage, the amplifier's input resistance sets the input current (*Iin*). Importantly, Kirchhoff's Current Law also tells us that the input current is the sum of the branch currents. From the perspective of the AC input, the branch current that flows through R_E and r_e is only the BJT's base current which is beta times smaller than the actual current through R_E and r_e. That being the case, from the perspective of the AC input, R_E and r_e appear to be beta times bigger than they really are.

Output resistance

Again, if you consider the circuit in Figure 5, the resistance between the two output terminals appears to be the simple parallel combination of R_C and the resistance of the current source in series with r_e and R_E. However, the ideal resistance of a current source is infinity and in practice usually very large. That being the case, the equation for the output resistance is:

$$Rout = R_C$$

Voltage gain

The equation for calculating the common emitter configuration's voltage gain is derived by applying a little algebra to the general equation for voltage gain: $Av_{(unloaded)} = \frac{Vout}{Vin}$.

If you consider the circuit in Figure 5, you can see that from an AC perspective the amplitude of the output signal must be the same as the amplitude of the AC voltage across the collector resistor. Using Ohm's Law, the AC voltage across the collector resistor is: $i_C \times R_C$.

Substituting $i_C \times R_C$ for *Vout* in the general gain equation gives: $Av_{(unloaded)} = \frac{i_C \times R_C}{Vin}$.

Similarly, it can be seen that the amplitude of the input signal must be the same as the amplitude of the AC voltage across the series combination of r_e and R_E. Again, using Ohm's Law, the AC voltage across both of these resistors is: $i_E \times (r_e + R_E)$.

Substituting $i_E \times (r_e + R_E)$ for *Vin* in the gain equation above gives: $Av_{(unloaded)} = \frac{i_C \times R_C}{i_E \times (r_e + R_E)}$.

Now, as the collector and emitter currents are almost equal, i_E in this equation can be substituted with i_C which gives: $Av_{(unloaded)} = \frac{i_C \times R_C}{i_C \times (r_e + R_E)}$.

Finally, simplifying this expression by cancelling out i_C gives:

$$Av_{(unloaded)} = \frac{R_C}{r_e + R_E}$$

Note: Test questions will not ask you to show how this equation is derived.

Practise calculating the AC parameters for a common emitter BJT amplifier by trying the following questions.

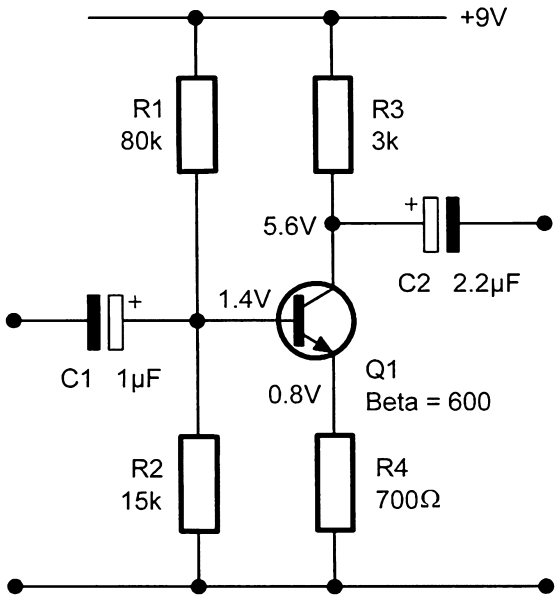

Figure 6

1. Calculate the amplifier's emitter current.

2. Calculate the BJT's dynamic emitter resistance (r_e).

3. Calculate the amplifier's input resistance.

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4. What is the output resistance?

5. Calculate the unloaded voltage gain.

6. Calculate the output signal's amplitude for a 200mVp-p input signal.

The effects of loading on the common emitter configuration

Recall from your work in and earlier amplifiers unit that when a load is connected to an amplifier's output, the size of the output signal and the voltage gain go down. This is equally true for transistor amplifier circuits.

To demonstrate this, consider the circuit in Figure 6 (on page 4-7). With 200mVp-p on the input you calculated that the amplifier's unloaded output voltage is 830mVp-p. So, let's see what the output voltage and gain would be if a 5kΩ load is connected to the amplifier.

One method of solving this is to use the equivalent amplifier model that you learnt about in an earlier subject as shown in Figure 7. The unloaded voltage gain, the output resistance and the unloaded output voltage (all of which you have just calculated) have been added to the model.

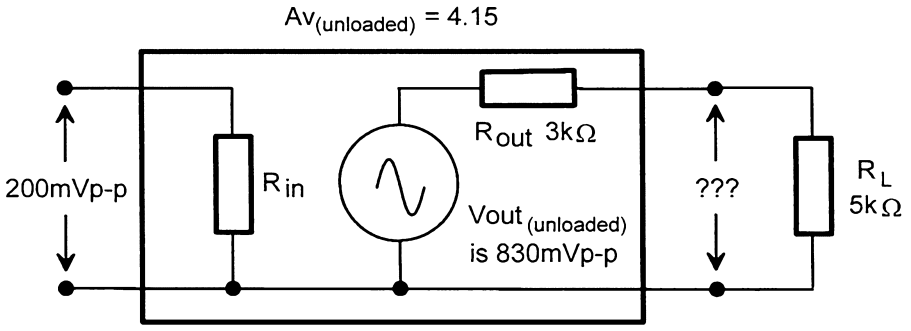

Figure 7 *The equivalent amplifier model for the circuit in Figure 6*

Recall that the loaded output voltage is found using $Vout_{(loaded)} = Vout_{(unloaded)} \times \frac{R_L}{Rout+R_L}$ and is calculated to be 519mVp-p (the working isn't shown here but you can check it for yourself).

Once the loaded output voltage is known, the loaded voltage gain is found using the equation $Av_{(loaded)} = \frac{Vout_{(loaded)}}{Vin}$ and is calculated to be 2.59 (again, the working isn't shown here but you can check it for yourself).

To understand the alternative method for finding the loaded voltage gain (which you're expected to use for this subject) consider the loaded amplifier's AC equivalent circuit in Figure 8 below.

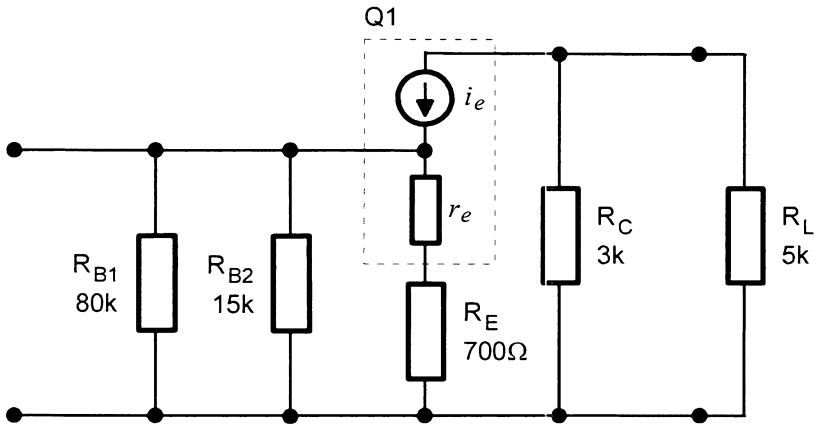

Figure 8 *The AC equivalent circuit of Figure 6 with a 5kΩ load connected*

The circuit makes it clear that the collector resistor and the load resistor are connected in parallel with each other. This means that the gain equation changes from $Av_{(unloaded)} = \frac{R_C}{r_e+R_E}$ to:

$$Av_{(loaded)} = \frac{R_C//R_L}{r_e+R_E}$$

So, if we use this equation to find the loaded voltage gain of the amplifier in Figure 6 with a 5kΩ load we get:

$$Av_{(loaded)} = \frac{R_C//R_L}{r_e+R_E}$$

$$Av_{(loaded)} = \frac{3k\Omega//5k\Omega}{22.75\Omega+700\Omega}$$

$$Av_{(loaded)} = \frac{1875\Omega}{722.75\Omega}$$

$$Av_{(loaded)} = 2.59$$

Notice that this is the same value of loaded gain that we found for the circuit using the equivalent amplifier model method.

Beware! A trap for beginners is to think that, because the load is connected in parallel with the collector resistor (according to the AC equivalent circuit), the amplifier's output resistance changes and becomes the parallel combination of the two resistors. This is not the case! The output resistance of the common emitter configuration is always the same as the resistance of the collector resistor - with or without a load connected.

The effects of by-passing the emitter resistor

The unloaded voltage gain of the circuit in Figure 6 (×4.15) is at the low end of the range of possible gains for the common emitter configuration. A simple modification can increase the gain dramatically and involves connecting a capacitor across the emitter resistor as shown in Figure 9 below. The capacitor is called the *emitter resistor by-pass capacitor* and is denoted in the circuit as C_E.

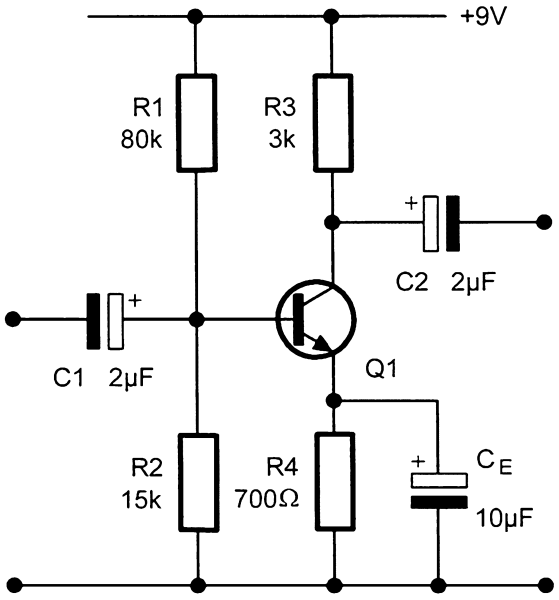

Figure 9 *The circuit of Figure 6 with a capacitor connected across the emitter resistor*

Capacitors look like an open-circuit to DC currents and so the inclusion of the emitter resistor by-pass capacitor has no effect on the circuit's quiescent DC conditions. However, as capacitors look like a short-circuit to the AC signals (provided the capacitor's value is big enough) the emitter resistor is by-passed. The effect of this on the AC equivalent circuit is shown in Figure 10 on the next page.

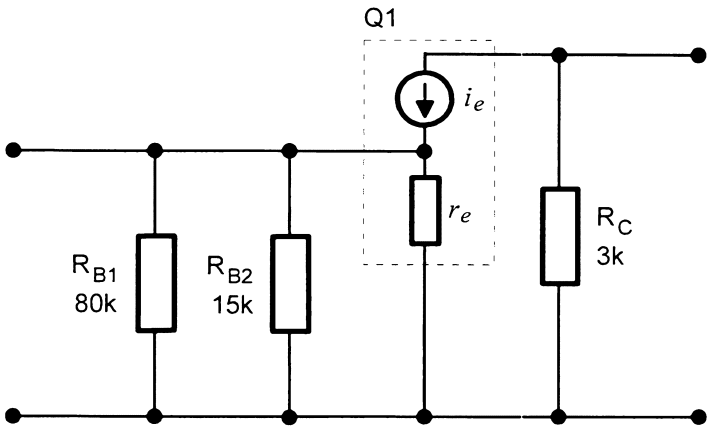

Figure 10 *The AC equivalent circuit of Figure 9*

Notice that R_E is missing. That being the case, when calculating the unloaded and loaded voltage gains for a common emitter BJT amplifier with an emitter resistor by-pass capacitor, R_E is removed from the equations as shown below.

$$Av_{(unloaded)} = \frac{R_C}{r_e}$$

$$Av_{(loaded)} = \frac{R_C // R_L}{r_e}$$

Mathematically, this change to the equations must result in higher values of gain.

For a more technical explanation, recall that the emitter resistor introduces negative feedback into the circuit (how it does so is explained later in this subject). The negative feedback is used to make the quiescent DC conditions around the circuit virtually independent of the BJT's beta and so make the circuit's DC operation more stable. It also helps to prevent a problem called *thermal runaway*.

However, recall that negative feedback lowers an amplifier's gain. While this might be fine for op amps with their unusably large open-loop voltage gains, the open-loop voltage gain of BJT amplifiers is much lower and so the negative feedback can lower the gain too much.

By-passing the emitter resistor with a capacitor offers the best of both worlds. The resistor is still visible to the DC circuit providing it with the necessary negative feedback and DC stability. However, the emitter resistor is not part of the AC circuit and so there is no AC negative feedback to lower the gain.

That said, there is a price. By-passing the emitter resistor and effectively removing it from the circuit has the unfortunate effect of reducing the size of the input resistance. This can be understood if you consider the new equation for calculating input resistance below. Notice that R_E is missing and without it the input resistance must be smaller.

$$Rin = R_{B1} // R_{B2} // \beta \times r_e$$

Practise using these equations by trying the following questions.

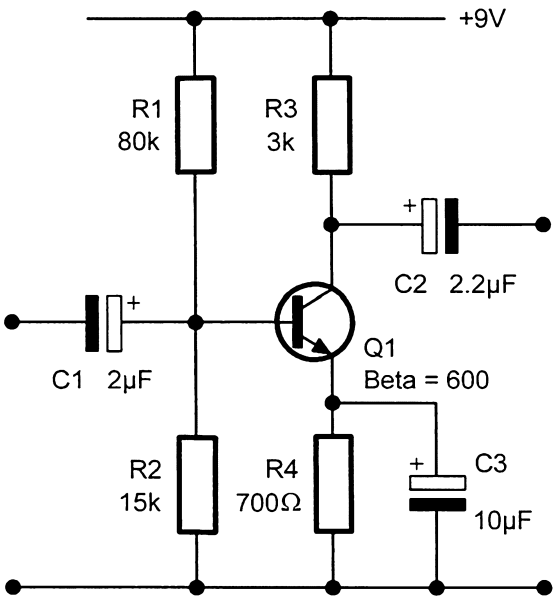

Figure 11

1. Calculate the amplifier's input resistance. [**Tip:** You've already calculated r_e because this is the circuit in Figure 6 on page 4-7.]

2. Calculate the unloaded voltage gain.

3. What is the loaded voltage gain if a 5kΩ load is connected across the output?

In some cases, the gain is too low without the emitter resistor by-pass capacitor and too high with it. The solution to this problem is to partially by-pass the emitter resistor by having two emitter resistors and using a capacitor to by-pass only one of them. This is shown in Figure 12.

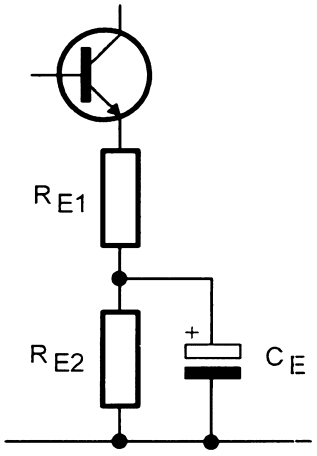

Figure 12 *The emitter resistor can be partially by-passed to so that there is some AC negative feedback*

In this circuit, both emitter resistors are providing DC negative feedback but only R_{E1} provides AC negative feedback (because is R_{E2} by-passed).

Common collector amplifier parameters

Consider the circuit in Figure 13 below. You should recognise that it's a voltage divider biased, common collector NPN BJT amplifier.

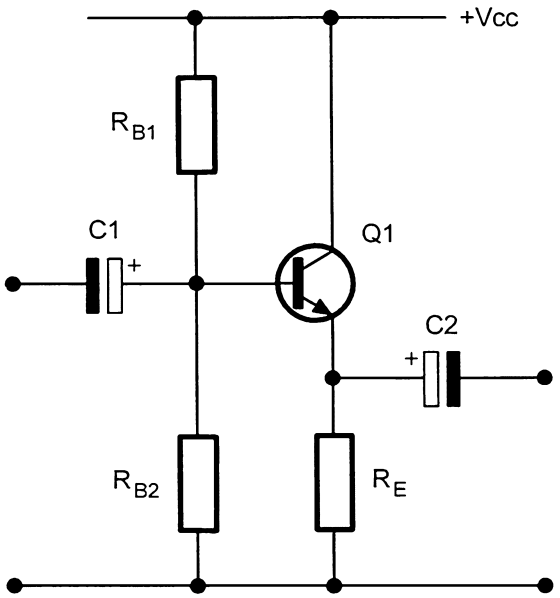

Figure 13 *A voltage divider biased common collector NPN BJT amplifier*

The circuit in Figure 14 below is the AC equivalent circuit of Figure 13. It has been developed by shorting all capacitors, shorting the power supply to common and replacing the BJT with its AC equivalent model.

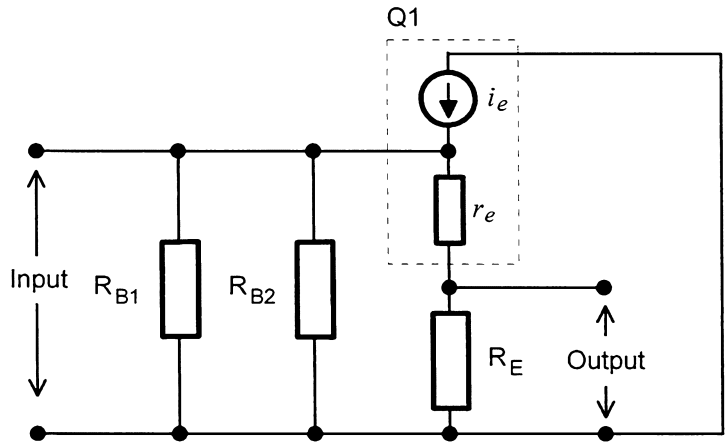

Figure 14 *The AC equivalent circuit for the common collector amplifier in Figure 13*

This circuit can now be used to help show how the equations for the AC parameters are derived. (**Note:** Test questions will not ask you to draw this circuit.)

Input resistance

If you consider the AC equivalent circuit in Figure 14 you can see that the arrangement between the input terminals of a common collector configuration is the same as for the common emitter configuration. That being the case, the equation for calculating the input resistance is the same and is shown again below:

$$Rin = R_{B1}//R_{B2}//\beta \times (R_E + r_e)$$

Output resistance

Again, if you consider the circuit in Figure 14, the resistance between the two output terminals appears to be the parallel combination of the emitter resistor (R_E) and the network formed by r_e in series with the parallel combination of the base resistors. However, there is a little more to it than this though because, looking back into the amplifier from the output, the total resistance of the parallel combination of the base resistors and the source's output resistance is smaller by a factor of beta.

That being the case, the equation for calculating the output resistance is: $Rout = R_E//(r_e + \frac{R_{B1}//R_{B2}}{\beta})$. If a source is connected to the amplifier's input (which is highly likely) the equation becomes: $Rout = R_E//(r_e + \frac{R_{B1}//R_{B2}//Rout_{(source)}}{\beta})$.

However, using a couple of simple assumptions, we can avoid having to use this equation! First, if the amplifier's source is ideal, its output resistance is zero. This reduces the equation to: $Rout = R_E//r_e$. And, as R_E is likely to be at least a few hundred Ohms, it will also be at least ten times bigger than r_e. This reduces the equation to:

$$Rout \approx r_e$$

Voltage gain

The equation for calculating the common collector configuration's voltage gain is derived by applying a little algebra to the general equation for voltage gain: $Av_{(unloaded)} = \frac{Vout}{Vin}$.

If you consider the diagram in Figure 14 you can see that, from an AC perspective, the amplitude of the output signal must be the same as the amplitude of the AC voltage across the emitter resistor. Using Ohm's Law, the AC voltage across the emitter resistor is: $i_E \times R_E$.

Substituting $i_E \times R_E$ for *Vout* in the general gain equation gives: $Av_{(unloaded)} = \frac{i_E \times R_E}{Vin}$.

Similarly, it can be seen that the amplitude of the input signal must be the same as the amplitude of the AC voltage across the series combination of r_e and R_E. Again, using Ohm's Law, the AC voltage across both of these resistors is: $i_E \times (r_e + R_E)$.

Substituting $i_E \times (r_e + R_E)$ for *Vin* in the gain equation above gives: $Av_{(unloaded)} = \frac{i_E \times R_E}{i_E \times (r_e + R_E)}$.

Finally, simplifying this expression by cancelling out i_E gives:

$$Av_{(unloaded)} = \frac{R_E}{r_e + R_E}$$

Note: Test questions will not ask you to show how this equation is derived.

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Practise calculating the AC parameters of the common collector configuration by trying the following questions.

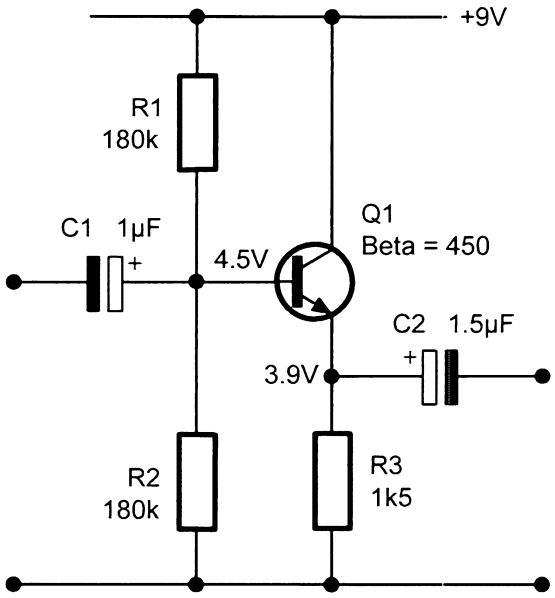

Figure 15

1. Calculate the amplifier's emitter current.

2. Calculate the BJT's dynamic emitter resistance (r_e).

3. Calculate the amplifier's input resistance.

4. Calculate the output resistance.

5. Calculate the unloaded voltage gain.

6. Calculate the output signal's amplitude for a 3Vp-p input signal.

The effects of loading on the common collector configuration

Although loading affects all voltage amplifiers, you may recall from your earlier work in amplifiers that the smaller the value of an amplifier's output resistance, the less effect that a load is likely to have on the amplifier's output voltage and voltage gain. The ideal voltage amplifier would have an output resistance of 0Ω and would be totally unaffected by loading.

As the output resistance of the common collector configuration is typically less than 100Ω it is safe to say that, for the purposes of this subject, the effect of connecting a load is so small that it can be ignored. That being the case, we can say that the loaded gain and input resistance are the same as the unloaded gain and input resistance.

Having said that, the common collector amplifier is used extensively in the output stage of power amplifiers which are required to drive very low resistance loads (for example, speakers) which will affect the voltage gain. However, when the circuit is used for this purpose its power gain is of much more importance that its voltage gain (as you will see later in this subject).

The effects of by-passing the emitter resistor

This heading is a red-herring because an emitter resistor by-pass capacitor is never used on the common collector configuration. The reason for this is simple: if one were connected it would short-circuit the output to common and there would be no output signal.

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Student notes

Skill practice 4

Practise measuring AC voltages in BJT amplifiers using an oscilloscope to determine input-output phase relationship, voltage gain and frequency response

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 1½ hours to complete this exercise.

Equipment

- Emona Trainer
- DMM
- BC549 transistor
- 100kΩ ¼W resistor
- two 22kΩ ¼W resistors
- 6k8Ω ¼W resistor
- 3k9Ω ¼W resistor
- 1kΩ ¼W resistor
- two 1µF capacitors
- 100µF capacitor
- three BNC to alligator-clip leads
- hook-up wire
- wire strippers

Remember:

Follow TAFE NSW WHS guidance at all times!

Work tasks

1. Read your WHS responsibilities at the top of the form below. Then conduct a WHS risk assessment and record your findings in the space provided.

Responsibilities of students under the Model WHS Act: s28

- Take reasonable care for your own health and safety by working safely at all times
- Take reasonable care to ensure that your acts or omissions don't put the health and safety of others at risk
- Follow all TAFE NSW WHS guidance and comply with all reasonable instructions from TAFE NSW staff to assist them in complying with the TAFE NSW WHS requirements
- In addition to the above, you must:
  - use and maintain machinery, tools and all other equipment properly and safely
  - ensure that your work area is free of hazards
  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

Risks involved in this activity include:	**Control measures:**
Trip hazards (eg students bags) Objects dropped on feet (while equipment is taken to and from workbenches).	Move bags and other objects from walkways Plan lifting of equipment
Others: _____	Other: _____
_____	_____
_____	_____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

3. Turn off the Emona Trainer then wire the circuit of Figure 1.

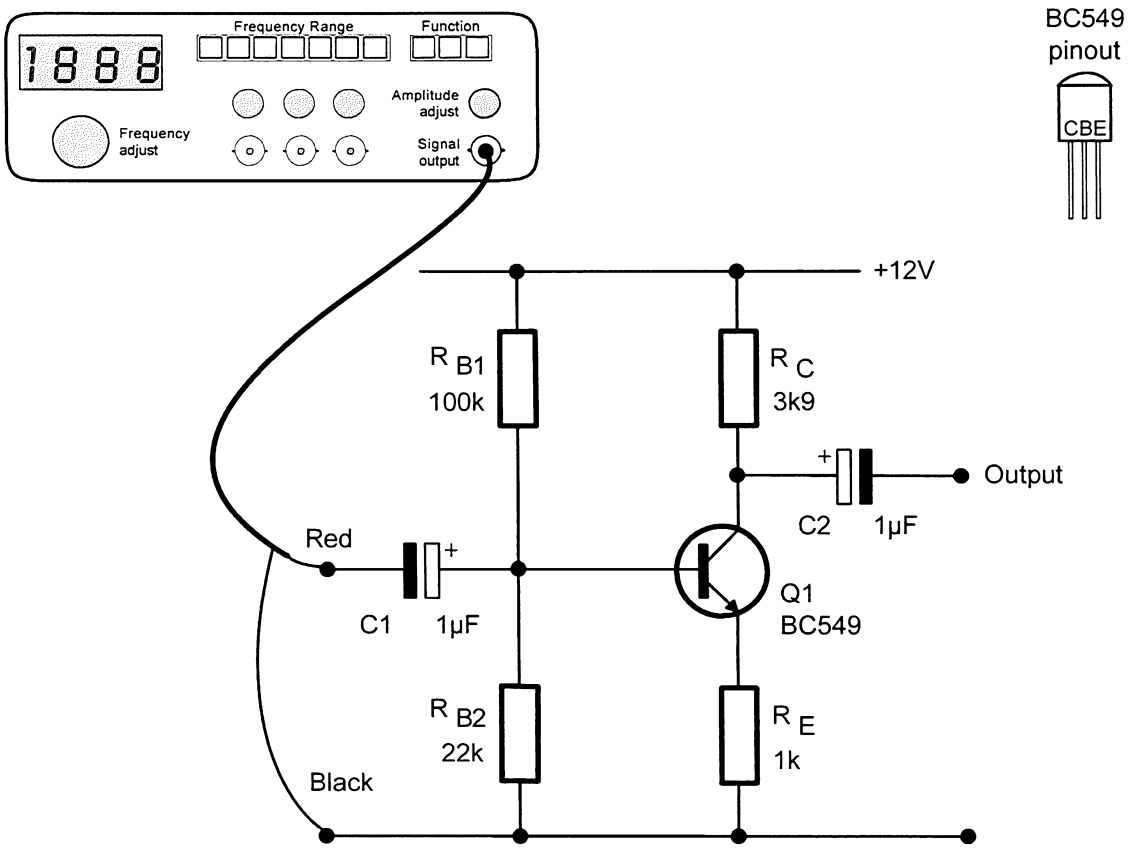

Figure 1

4. Switch on the Emona Trainer but **don't** switch on the signal generator.

5. Measure the base-emitter voltage with the DMM.

   Self check: If the base-emitter voltage (V_{BE}) is between 0.55V and 0.7V then your circuit is probably working so go to Step 6. If V_{BE} is not within this range then there is probably something wrong with the circuit. Check your wiring but if you still can't get the circuit working, call the teacher.

6. Measure the emitter voltage (V_E).

   V_E = _____

7. Calculate the emitter current (I_E).

   _____

   _____

8. Calculate the BJT's r_e using the equation: $r_e = \frac{26mV}{I_E}$.

   _____

   _____

9. Calculate the amplifier's theoretical voltage gain using the equation: $Av = \frac{R_C}{r_e+R_E}$. Record this value in the appropriate space in the first row of Table 1 (on the next page).

10. Turn on the signal generator.

11. Connect the CRO's channel 1 input to the amplifier's input.

12. Set the signal generator to produce a 1kHz sinewave at 1Vp-p.

13. Connect the CRO's channel 2 input to the amplifier's output.

14. Measure and record the output signal's amplitude (that is, its peak-to-peak voltage).

15. Calculate and record the gain using your measured input and output voltages.

16. Observe and record the phase relationship between the input and output signals.

Table 1	Theoretical gain	Output voltage	Measured gain	Phase relationship
Circuit as shown in Figure 1				
With the load resistor				
With the load and by-pass capacitor				

The teacher needs to check your work at this point...

17. Connect a 6k8Ω resistor across the amplifier's output terminals.

18. Calculate the amplifier's new theoretical voltage gain using the equation: $Av = \frac{R_C // R_L}{R_E + re}$. Record this in the appropriate space in the middle row of Table 1.

19. Check that the input voltage is still 1Vp-p. If not, readjust it.

20. Repeat steps 14 to 16.

21. With the load resistor still connected, use the 100µF capacitor to by-pass the emitter resistor. Be sure to connect the capacitors positive leg to the emitter and the negative leg to ground.

22. Set the signal generator to 40mVp-p (still at 1kHz).

23. Calculate the amplifier's new theoretical voltage gain using the equation: $Av = \frac{R_C // R_L}{re}$. Record this in the appropriate space on the bottom row of Table 1.

24. Repeat steps 14 to 16.

The teacher needs to check your work at this point...

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Question 1
What is the typical range of gain for this configuration? Are the measured gains for your circuit within this range?

Question 2
What is the theoretical input-output phase relationship for this configuration? Is the phase relationship of your circuit correct?

Question 3
What happened to the amplifier's gain when the load resistor was connected? Why?

Question 4
What happened to the amplifier's gain when the emitter resistor by-pass capacitor was connected? Why?

25. Measure the circuit's *f1*. Record the frequency in Table 2 on the next page.

    Tip: The *f1* point is that lower frequency where the output voltage has dropped to 0.707 of the output voltage at a mid-band frequency.

26. Measure and record the circuit's *f2*.

    Tip: The *f2* point is that higher frequency where the output voltage has dropped to 0.707 of the output voltage at a mid-band frequency.

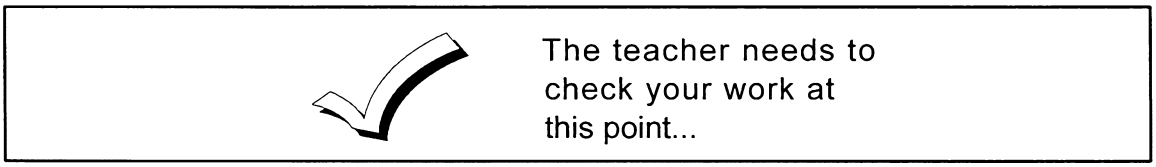
27. Calculate and record the amplifier's bandwidth.

Table 2

f1 frequency	*f2* frequency	Bandwidth

Question 5

Based your amplifier's frequency performance, can it be used to amplify signals in the audio range of frequencies? Explain your answer.



28. Turn off the Emona Trainer and the signal generator.

29. Rewire the circuit as shown in Figure 2.

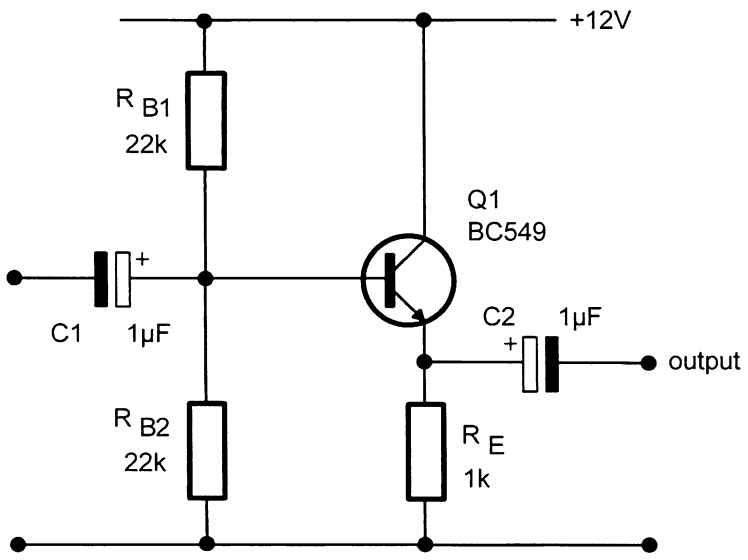


Figure 2

30. Turn on the Emona Trainer.

31. Measure the base-emitter voltage with the DMM.

    Self check: If the base-emitter voltage (V_{BE}) is between 0.55V and 0.7V then your circuit is probably working so go to Step 32. If V_{BE} is not within this range then there is probably something wrong with the circuit. Check your wiring but if you still can't get the circuit working, call the teacher.

32. Measure the emitter voltage (V_E).

    V_E = _____

33. Calculate the emitter current (I_E).

    _____

    _____

34. Calculate the BJT's r_e.

    _____

    _____

35. Calculate the amplifier's theoretical voltage gain using the equation: $Av = \frac{R_E}{re+R_E}$. Record this in the appropriate space in the top row of Table 3 (on the next page).

36. Connect the signal generator to the circuit and turn it on.

37. Connect the CRO's channel 1 input to the amplifier's input.

38. Set the signal generator to produce a 1kHz sinewave at 1Vp-p.

39. Connect the CRO's channel 2 input to the amplifier's output.

40. Measure and record the output signal's amplitude using the CRO.

41. Calculate and record the gain using your measured input and output voltages.

42. Observe and record the phase relationship between the input and output signals.

Table 3	Theoretical gain	Output voltage	Measured gain	Phase relationship
Circuit as shown in Figure 2				
With the load resistor				

The teacher needs to check your work at this point...

43. Connect a 6k8Ω resistor across the output terminals.

44. Check that the input voltage is still 1Vp-p. If not, readjust it.

45. Repeat steps 40 to 42.

Question 6
What is the typical gain for this configuration? Is the gain for your circuit correct?

Question 7
What is the theoretical input-output phase relationship for this configuration? Is the phase relationship of your circuit correct?

Question 8
Why didn't the amplifier's output voltage drop when the load was connected?

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The teacher needs to check your work at this point...

46. Measure the circuit's *f1*. Record the frequency in Table 4 below.

    Tip: Remember that to find *f1* you reduce the frequency of the amplifier's input signal until the amplitude of the output voltage drops to 0.707 of its mid-band output voltage.

    Another tip: Before you adjust the frequency of the input signal, make things easier for yourself by first adjusting its amplitude so that the amplifier's output is seven divisions peak-to-peak (and not clipped).

47. Measure and record the circuit's *f2*.

    Tip: Remember that to find *f2* you increase the frequency of the amplifier's input signal until the amplitude of the output voltage drops to 0.707 of its mid-band output voltage.

48. Calculate and record the amplifier's bandwidth.

Table 4

***f1* frequency**	***f2* frequency**	**Bandwidth**

The teacher needs to check your work at this point...

Review questions

Answer these questions to check your understanding of what you have learnt for this chapter. Doing this will also help to prepare you for the tests.

Questions 1 to 13 refer to the circuit of Figure 1

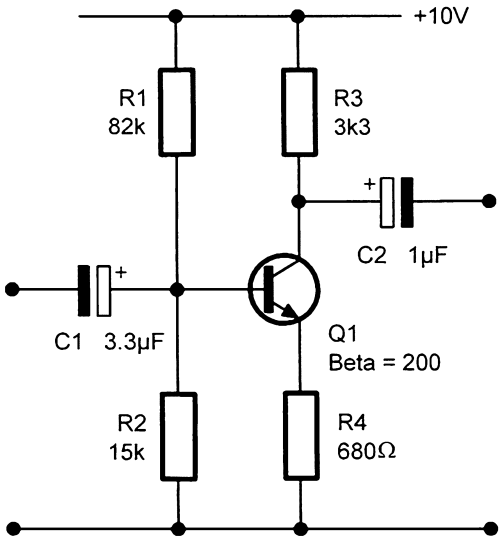

Figure 1

1. Calculate the base voltage (V_B).

2. Calculate the emitter voltage (V_E).

3. Calculate the collector voltage (V_C).

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4. Calculate the BJT's dynamic emitter resistance (r_e).

5. Calculate the amplifier's unloaded voltage gain ($Av_{(unloaded)}$).

6. Calculate the input resistance (*Rin*).

7. What is the output resistance (*Rout*)?

8. What is the phase relationship between the input and output signals?

9. Determine the maximum peak-to-peak output voltage before clipping.

10. Calculate the maximum peak-to-peak input voltage before clipping appears at the output.

11. What would be the effect on the voltage gain if *R3* was substituted for an 8kΩ resistor?

12. What would be the effect on the voltage gain if *R4* was substituted for a 1kΩ resistor?

13. What would be the effect on the voltage gain if the BJT was substituted for a similar BJT with a beta of 350? Explain your answer.

Questions 14 to 24 refer to Figure 2

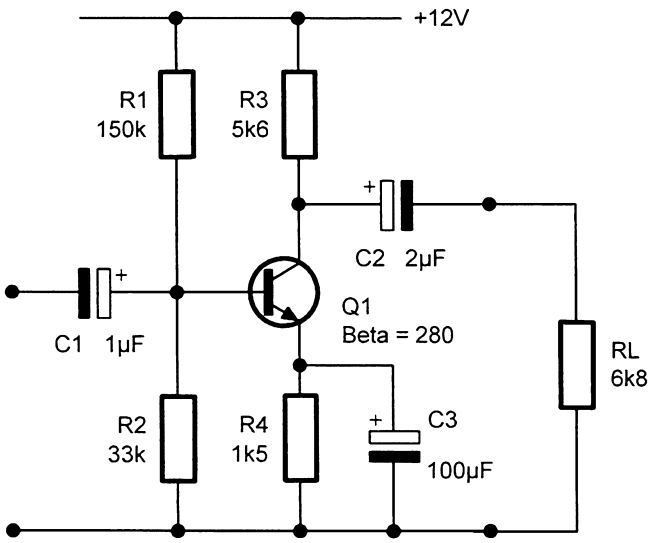

Figure 2

14. Calculate the base voltage (V_B).

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15. Calculate the emitter voltage (V_E).

16. Calculate the collector voltage (V_C).

17. Calculate the BJT's dynamic emitter resistance (r_e).

18. Calculate the amplifier's loaded voltage gain ($Av_{(loaded)}$).

19. Calculate the input resistance (*Rin*).

20. What is the output resistance (*Rout*)?

21. Calculate the input voltage that will develop a 9Vp-p output voltage.

22. What would be the effect on the output signal if R_L went open circuit? Why?

23. What would be the effect on the output signal if *C3* went open circuit? Why?

24. What would be the effect on the input resistance if *C3* went open circuit? Why?

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Questions 25 to 28 refer to the circuit of Figure 3

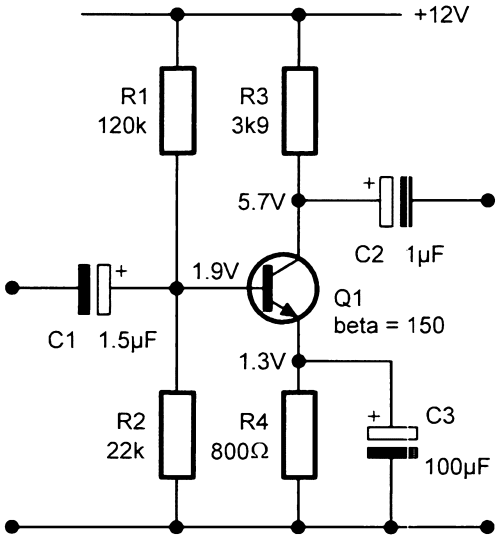

Figure 3

25. Calculate the BJT's dynamic emitter resistance (r_e).

26. Calculate the amplifier's unloaded voltage gain ($Av_{(unloaded)}$).

27. Calculate the input resistance (*Rin*).

28. What would be the effect on the collector current if *C3* went open-circuit? Why?

Questions 29 to 34 refer to the circuit in Figure 4

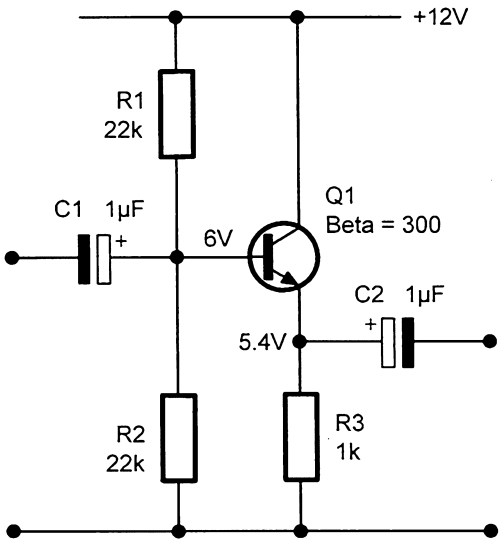

Figure 4

29. Calculate the BJT's dynamic emitter resistance (r_e).

30. Calculate the amplifier's unloaded voltage gain ($Av_{(unloaded)}$).

31. Calculate the input resistance (*Rin*).

32. Calculate the output resistance (*Rout*).

33. What is the phase relationship between the input and output signals?

34. What would happen to the amplifier's voltage gain if a 1kΩ load was connected? Explain your answer.

Question 35 refers to the circuit in Figure 5 below

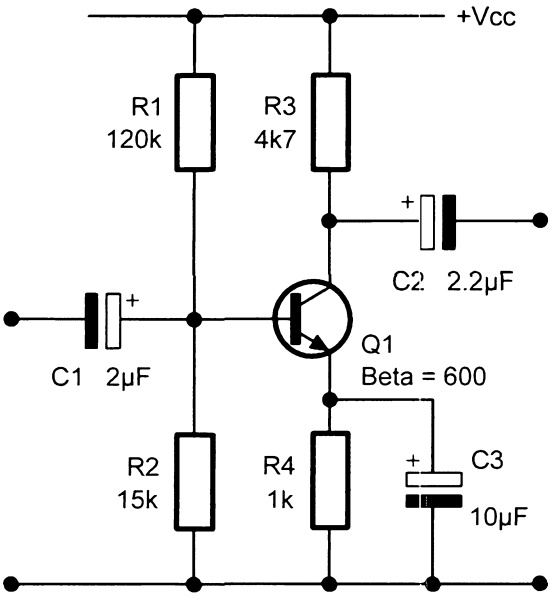

Figure 5

35. Calculate the BJT's base voltage if the measured output signal is 293 time bigger than the measured input signal.

Section 5 Fault-finding BJT amplifier circuits and testing BJTs

Purpose To develop your knowledge and ability to test BJT circuits and BJTs and to choose suitable replacements for faulty BJTs.

Objectives At the end of the lesson you should be able to:

- List the changes to AC signals around BJT amplifier circuits that indicate the likely presence of a fault
- Predict the effect on the quiescent DC voltages of a BJT amplifier circuit for given faults
- Use fault symptoms to identify the specific problem in a faulty a BJT amplifier circuit
- Test BJTs for faults using a digital multimeter
- Use manufacturers' data sheets to look up relevant DC terminal characteristics of BJTs
- Choose a replacement BJT using manufacturers' data

Introduction

The purpose of the Certificate III in Electronics & Communications is to teach students about electronics theory to help them repair electronics equipment to component level (that is, down to finding which component is causing the fault and replacing it if possible). This chapter focuses on taking what you have learnt so far about BJT amplifier circuits and showing you how to use it to find faults.

Recognising a faulty BJT amplifier circuit

To test any amplifier circuit for faults, you must connect an appropriate input signal to it, power the circuit up, then use the a CRO to look at its input and output. You've actually been practising doing that in the previous two practical exercises (ie the exercises in Sections 3 and 4).

When you look at the amplifier's input, you check that there's actually a signal there and you examine the signal's shape and measure its size. Next, you look at the amplifier's output and do the same. Finally, you compare the amplifier's input and output and look for one of the following:

- the output signal is smaller than it should be
- the output signal is bigger than it should be
- there's no output signal at all
- the output signal is clipped (when it shouldn't be for the size of the input signal)
- the output signal is distorted in some other way
- the output signal has the incorrect phase relationship with the input signal

Any of these problems would be considered "symptoms" of a potential fault with the circuit. (Though, the fault may be with the circuit's load causing it to perform incorrectly.)

Locating the specific problem

Once you've established that a BJT amplifier circuit is faulty, it can be useful to perform a visual inspection of the circuit to look for things like:

- burnt components (these may smell too)
- broken printed circuit board (PCB) tracks or wires
- dry solder joints and solder-dags they may be causing short-circuits
- excessive solder flux
- buzzing, humming or sizzling sounds that can identify the faulty component

Identifying and correcting any of these problems may fix the amplifier. If it doesn't, or you didn't notice any of these problems, the next step does **not** involve removing each of the components in the circuit and testing them. Doing this might seem like a good trouble-shooting strategy, especially if there are only a handful of components. However, there are several problems with it. First, it's inefficient and there are faster ways of identifying the specific problem. Second, there's a very real risk of damaging the printed circuit board when desoldering and resoldering components so this should be kept to a minimum. Third, you may introduce problems by accidentally putting components back in the wrong polarity or by damaging a component due to ESD or overheating during the de-soldering and re-soldering process.

So what's the next step? You measure the quiescent DC voltages around the circuit as explained in Section 2. This is useful to do because most faults upset the DC voltages around the circuit. If you find that one or more voltages have changed, there's likely a problem. Better still, the way the voltage or voltages have changed can tell you which component is faulty and what's wrong with it.

The quiescent DC voltages that you measure are:

- the power supply voltage (Vcc)
- the common rail voltage
- the transistor's collector voltage (V_C)
- the transistor's base voltage (V_B)
- the transistor's emitter voltage (V_E)
- the transistor's base-emitter voltage (V_{BE})

There are a few important points to make about this. First, although you will have checked the power supply earlier in the fault-finding process, if you have found that it's ok, it doesn't automatically mean that its voltage is reaching all the components that it should. A cracked track that's not easily visible can prevent the supply voltages reaching all circuits and sometimes the cracks are too fine to see with the naked eye. So, you should measure the Vcc on the leg of every component connected to it.

Second, it may seem silly to measure the common rail's voltage (wouldn't it be zero?!) but again a cracked track can prevent the common reaching all circuits. Without a common, the current path isn't closed and so no current flows in that path. You can suspect a cracked common track if its voltage is something other than 0V.

Third, you can only measure quiescent DC voltages when there's no input signal to the amplifier stage. So, you'll have to disconnect the source from the amplifier's input. If that's not possible, you may have to de-solder the circuit's input coupling capacitor to isolate it from its input.

Fourth, when you measure the quiescent DC voltages it can be helpful to compare them to what they should be. If this information isn't written on the schematic diagram, you can calculate the theoretical values. That said, the following is an excellent guide for what you would be looking for without the need to perform calculations:

- the collector voltage (V_C) should be somewhere around half of *Vcc* (anything from 40% to 60% of *Vcc* can be ok)
- the base voltage (V_B) should roughly be between 10% and 20% of *Vcc*
- the emitter voltage (V_E) should be about 0.6V less than the base voltage (V_B) - NPN
- the base-emitter voltage (V_{BE}) should be about 0.6V

Fifth, remember that the measured quiescent DC voltages can vary from theoretically predicted values due to tolerances of the resistors and the transistor's actual base-emitter forward voltage drop (remember, it can range from about 0.5V to 0.7V).

Component faults

To be able to effectively fault-find any electronics circuit, it's important to have a clear understanding of the typical faults that the components in the circuit can have. Below is a list of the most common faults experienced by the components in small signal BJT amplifier circuits. Of course, other faults are possible but they represent a small minority and so they're not dealt with here.

Component	Typical faults
Low power resistors (ie <2W)	■ High in value ■ Open-circuit
Electrolytic caps (aluminium oxide)	■ Open-circuit ■ Leaky
Ceramic and polyester caps	■ Open-circuit ■ Short-circuit
The p-n junction (diodes)	■ Open-circuit anode-cathode ■ Short-circuit anode-cathode
Bipolar junction transistors (BJTs)	■ Short-circuit collector-emitter ■ Short-circuit base-emitter ■ Short-circuit base-collector ■ Open-circuit collector ■ Open-circuit base ■ Open-circuit emitter

The effects of faults on the DC voltages around BJT circuits

As already mentioned, faults in BJT circuits usually upset the quiescent DC voltages around the circuit. Importantly, with a good understanding of BJT theory and knowledge of how BJTs and other components typically fail, it's usually possible to work out which component is faulty from the voltage measurements that you take.

The following is a list of some of the likely component faults and their effects on the DC quiescent voltage levels around a voltage divider biased BJT circuit.

- *Q1* open-circuit collector

  If the BJT's collector is open-circuit, there is no-longer a path for collector current to flow. With no collector current, there's no potential difference across the collector resistor and so the voltage on the BJT's collector equals the supply voltage.

  At the same time, the lost transistor-action means that the combined resistance of base-emitter's p-n junction and the emitter resistor are now seen in parallel with R_{B2}. So, the base voltage goes down to a value that depends on component values. The voltage on the emitter is 0.6V less than the new base voltage.

- *Q1* open-circuit emitter

  If the BJT's emitter is open-circuit, there is no-longer a path for either the base or collector currents. This means that the voltage on the BJT's emitter is 0V and the voltage on the collector equals the supply voltage. However, the voltage on the base is largely unaffected.

- *Q1* open-circuit base

  If the BJT's base is open-circuit, there's no-longer a path for the base current and, with no base current, there is no collector current. This has the same effect on the DC voltages as the BJT with an open-circuit emitter (which means that you can't tell these two faults apart in-circuit but that's not a problem - the BJT is faulty and needs to be replaced).

- *Q1* short-circuit base-emitter

  If the BJT's base and emitter terminals are short-circuit they'll have the same voltage but it'll probably be lower than the voltage that is normally on either terminal. At the same time, the transistor-action is lost and so there'll no-longer be any collector current. This means that the voltage on transistor's collector equals the supply voltage.

- *Q1* short-circuit collector-emitter

  If the BJT's collector and emitter terminals are short-circuit they'll have the same voltage and it'll probably be similar to (but not the same as) the voltage that is normally on the emitter. The voltage on the base is likely to remain unaffected but this will depend on component values.

  The voltage on the collector and emitter terminals can be easily calculated because the collector and emitter resistors end up forming a simple voltage divider with this fault.

- *Q1* short-circuit collector-base

  If the BJT's base and collector terminals are short-circuit they'll have the same voltage but it'll be higher than the voltage that is normally on the base. The voltage on the emitter is 0.6V less than the new base voltage.

- R_{B1} high

  If R_{B1} is high in value, the voltage on the base is lower than normal. The voltage on the emitter is 0.6V less than the new base voltage and the voltage on the collector is higher than normal as a result.

- R_{B1} open-circuit

  If R_{B1} is open-circuit, the voltage on the base is 0V. The BJT is cut-off and so the voltage on the emitter is 0V and the voltage on the collector equals the supply voltage.

- R_{B2} high

  If R_{B2} is high in value, the voltage on the base is higher than normal. The voltage on the emitter is 0.6V less than the new base voltage and the voltage on the collector is lower than normal as a result.

- R_{B2} open-circuit

  If R_{B2} is open-circuit, the voltage on the base is probably different. The voltage on the emitter is 0.6V less than the new base voltage and the voltage on the collector is lower than normal if the emitter is higher than normal and vice versa.

- R_E high

  If R_E is high in value, the current through it is lower than normal and so the potential difference across R_C is smaller. This means that the voltage on the collector is higher than normal but the voltage on the base and emitter are unaffected.

- R_E open-circuit

  If R_E is open-circuit, there is no-longer a path for the base and collector currents to flow. As such, the voltage on the collector equals the supply voltage and the base voltage is unaffected.

  Theoretically, this should also mean that the emitter voltage is floating. However, connecting a voltmeter to the circuit to measure V_E connects a high value resistor (the meter's internal resistance) between the emitter and common. As a consequence, the base-emitter p-n junction can become forward biased. But, the emitter current is so small that the emitter voltage is likely to be smaller than 0.6V less than the base voltage.

- R_C high

  If R_C is high in value, the potential difference across it is greater than normal and so the voltage on the collector is lower than normal. The voltage on the base and emitter are unaffected.

- R_C open-circuit

  If R_C is open-circuit there is no-longer a path for the collector current to flow. The effect of this on the circuit voltages is similar to the effects of BJT with an open-circuit collector. The difference is, the collector voltage floats instead of equalling the supply voltage.

Note: Although you can be tested on fault-finding BJT amplifier circuits (and the others that you'll learn about in this subject) it's not advisable to memorise the effects of these faults. If you have a good understanding of BJT operation and the operation of the biasing circuits, you can work these out with practise.

Transistor faults

Many faults in amplifiers and other transistor circuits are caused by one or more of the transistors becoming faulty due to: ESD, equipment misuse, other faults in the circuit, voltages and currents momentarily exceeding maximum ratings, old age, overheating with a soldering iron, accidental shorting-out by a clumsy technician and so on. Whatever the cause, you'll change many transistors in your career as an electronics technician (assuming you're repairing equipment to component level).

Obviously, before you change a transistor you need to be certain that it's faulty. This isn't as hard as it might seem because the BJT's construction includes two p-n junctions. So, the procedure for testing BJTs is almost identical to the procedure for testing that other important p-n junction device, the diode.

Testing diodes

Diodes can be tested with analog multimeters (AMMs) using the ohmmeter function on the ×100 range (or equivalent). However, the ohmmeter function on most digital multimeters (DMMs) can't provide enough current to forward bias a p-n junction. So, DMM manufacturers usually provide a special diode test facility (often denoted by a the schematic symbol for a diode).

The DMM's diode test facility connects a current source between its probes as well as a voltmeter to measure the current source's potential difference. This is shown in Figure 2 below.

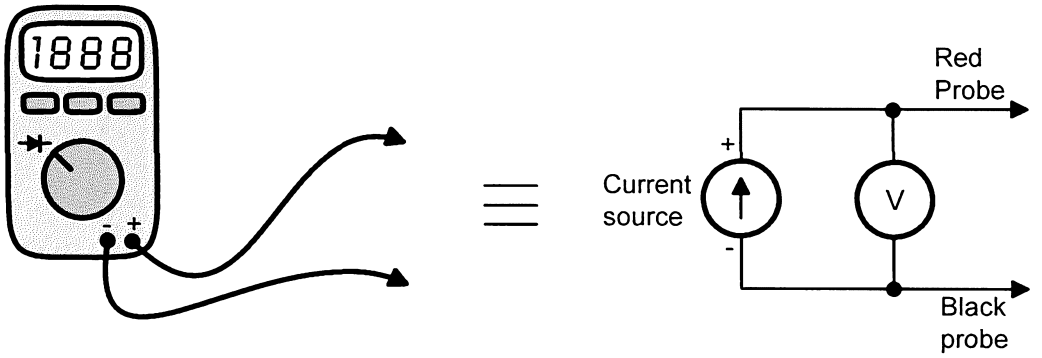

Figure 2 *The equivalent circuit of a DMM when set to the diode test mode*

If the DMM's leads are left open-circuit, the current source's output is zero amps and its potential difference is maximum. If the meter probes are shorted, the output current is maximum and its potential difference is zero volts.

Checking a diode simply involves performing the following tests in either order:

- Connect the DMM to the diode as shown in Figure 3a below. This reverse biases the diode so, if it's working normally, the meter displays the diode test's open-circuit reading. This is usually "OL" but some meters show a figure of about 2.8V.

- Connect the DMM as shown in Figure 3b below. This forward biases the diode so if it's working normally the meter displays the diode's forward voltage drop (which can be anything from about 0.5V to 0.7V).

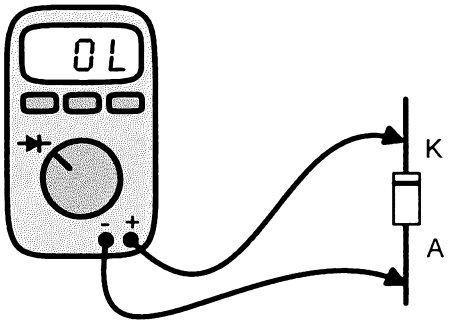

Figure 3a *Reverse biasing a working diode in this way gives the meter reading shown*

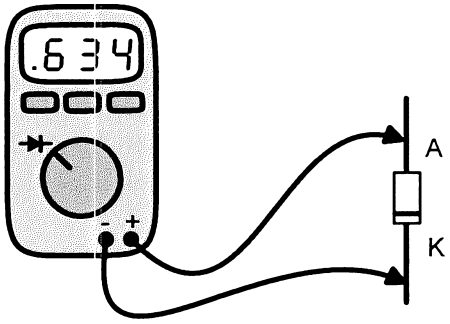

Figure 3b *Forward biasing a working diode in this way gives the meter reading shown*

There are two basic faults that the diode test facility on DMMs can detect.

1. Open-circuit anode-cathode

   For this fault the DMM reads high in both directions as shown in Figure 4 below.

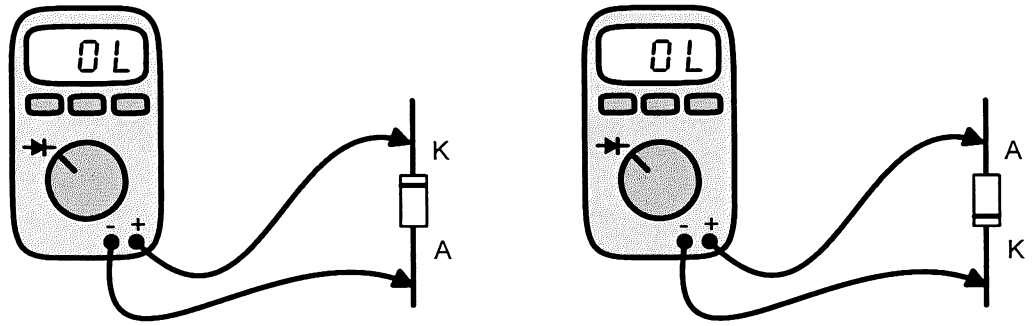

Figure 4 *The meter readings for both DMM connections when the diode is open-circuit*

2. Short-circuit anode-cathode

   For this fault the DMM reads zero volts in both directions as shown in Figure 5 below.

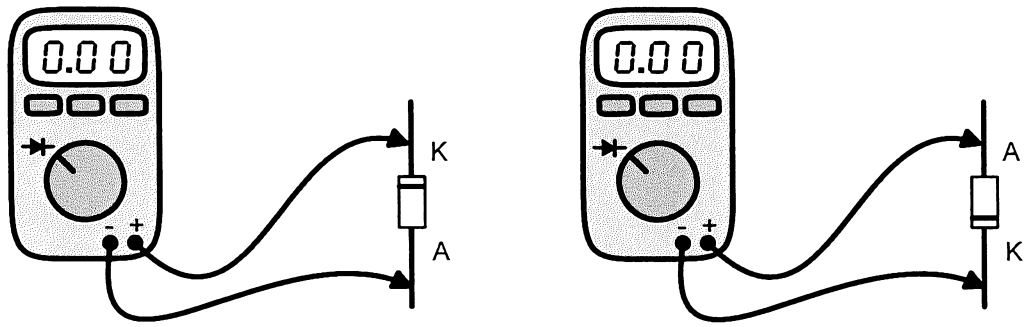

Figure 5 *The meter readings for both DMM connections when the diode is short-circuit*

Testing BJTs

The trick to testing BJTs involves thinking about them as diodes using the two-diode representative model introduced in Section 1. Recall that an NPN and PNP BJT can be thought of as two diodes connected back-to-back as shown in Figure 6 below.

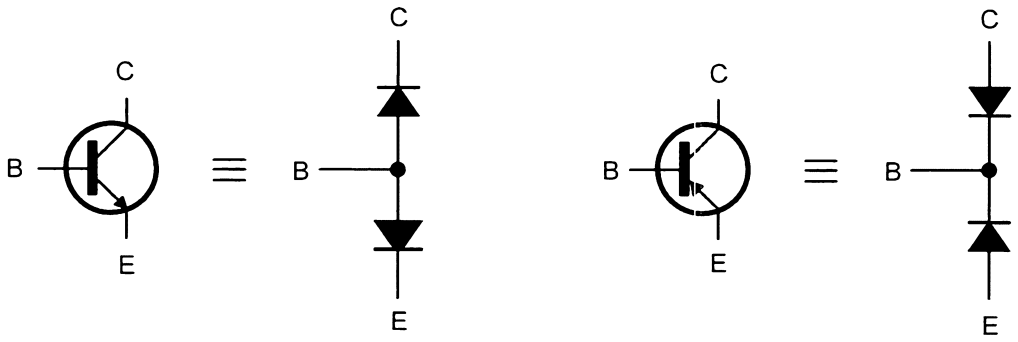

Figure 6 *The two-diode representative models for the NPN and PNP BJTs*

There are three sets of measurements that must be taken to test a BJT and two of them involve testing the base-collector and base-emitter p-n junctions just as though they're diodes. Figure 7 summarises the measurements and their readings for functional NPN and PNP BJTs. If readings are obtained other than the ones shown then the BJT may well be faulty.

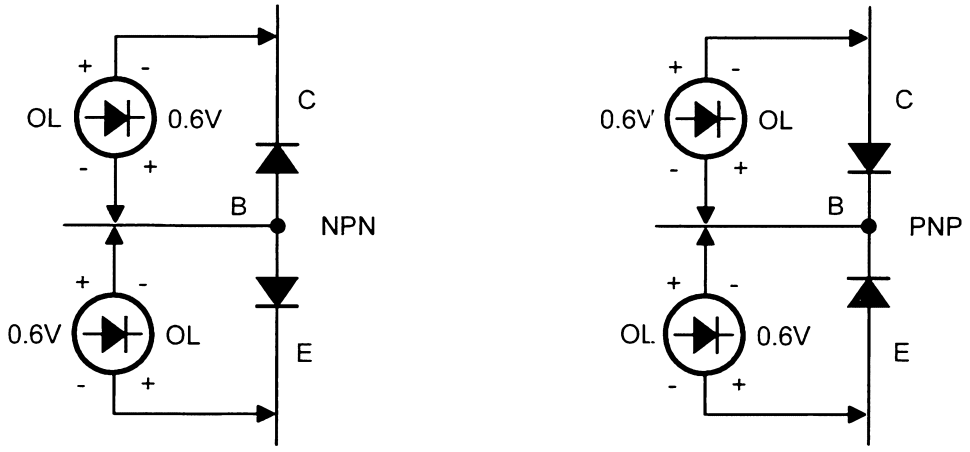

Figure 7 *A summary of the measurements needed to test the base-collector and base-emitter junctions of an NPN and PNP BJT*

The third set of measurements involves testing the BJT's collector-emitter connection. As the "diodes" between the collector and emitter are connected back-to-back it is impossible for current to flow in either direction (without a base current that is). That being the case, the DMM reads high in both directions as shown in Figure 8 below.

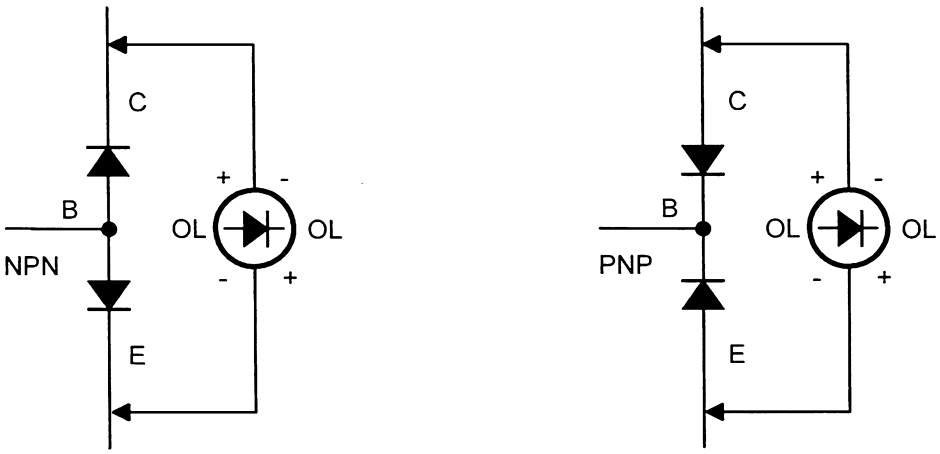

Figure 8 *A summary of the measurements needed to test the collector-emitter connection of an NPN and PNP BJT*

[Note: In the unlikely even that you're testing BJTs using an analog multimeter on the ×100 ohms range there is something important you must know. The black probe on most analog ohmmeters connects to the battery's positive terminal and the red lead to its negative terminal. This means that, when testing BJTs with an AMM, the polarities in Figures 7 and 8 must be reversed.]

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Identifying the transistor's terminals

Most (if not all) semiconductor companies publish data about their transistors. The datasheet for each device includes its part number, the package (or case), the pinout, and relevant electrical specifications. That being the case, identifying which of a transistor's terminals is the base, emitter and collector these days is easy - You just search for the device's datasheet on the internet.

When you do, type the transistor's part number (eg BC549) followed by the term "datasheet pdf" (so, your search might look like *BC549 datasheet pdf*) into your preferred search engine and you should get a match. Alternatively, you can visit the Element-14 or Mouser websites, type the transistor's part number into the search field and you'll get a bunch of hits with links to data sheets. This option can be better sometimes as it cut down on false matches.

Table 1 is a summary of this information for some of the commonly available transistors in this country.

Table 1

TYPE	CASE	N/P	V_{CE}	V_{CB}	I_C (A)	BETA	F_T	POWER	USE
BC548	TO-92*	N	30	30	0.1	110-800	300	0.5	SS amp
BC549	TO-92*	N	30	30	0.1	200-800	300	0.5	Low noise SS amp
BC559	TO-92*	P	30	30	0.1	125-600	150	0.5	SS amp
BC327	TO-92*	P	45	50	0.8	100-600	100	0.8	Output
BC337	TO-92*	N	45	50	0.8	100-600	200	0.8	Output
BD639	TO-92*	N	80	100	1	40-160	130	1	Audio output
BD640	TO-92*	P	80	100	1	40-160	50	1	Audio output
BD139	TO-126	N	60	100	1	40-160	250	8	Output
BD140	TO-126	P	80	100	1	40-160	75	8	Output
BF180	TO-72*	N	20	30	0.02	13	675	0.15	UHF amp
BF469	TO-126	N	250	50	0.5	50	60	1.8	High voltage amp
BF470	TO-126	P	250	250	0.05	50	60	1.8	High voltage amp
MJE2955	TO-220	P	60	70	10	20-100	2	75	Power
MJE3055	TO-220	N	60	70	10	20-100	2	75	Power
MJ2955	TO-3	P	60	70	15	20-70	4	115	High output power
2N3055	TO-3	N	60	90	15	20	0.8	115	High output power
MJ15003	TO-3	N	140	140	20	25-150	2	250	High output power
MJ15004	TO-3	P	140	140	20	25-150	2	250	High output power

* There is more than one variation of this package.

Key

N/P N = NPN and P = PNP

V_{CE} maximum collector-emitter voltage (volts)

V_{CB} maximum collector-base voltage (volts)

I_C maximum collector current (amps)

F_T maximum (transition) frequency (MHz)

POWER maximum power dissipation (watts)

SS amp small signal amplifier

UHF amp ultra-high frequency amplifier

Replacing fault transistors

Technicians usually replace faulty transistors (both BJTs and FETs) using either:

- the correct part;
- a suitable substitute identified in a cross-reference; or
- a suitable substitute identified by comparing transistor data.

Replacing a faulty transistor with the correct part

Unless there is a history of a particular transistor failing in a piece of equipment, replacing the faulty device with the correct part makes the most sense. It gives you the most confidence that the replacement will last.

However, it's not always easy to obtain the correct part. If your local parts supplier doesn't sell the transistor you need, try:

- Larger electronic parts suppliers (such as Element-14, WES Components)
- The manufacturer of the equipment the transistor is from (or their local distributor)
- A parts supplier overseas (via the internet)
- The manufacturer of the transistor (the part-number and manufacturer's logo may give a clue about who makes it)

Replacing a faulty transistor with a substitute identified in a cross-reference

Eventually, you are going to repair a piece of old equipment with a faulty transistor that is no-longer manufactured. When this happens, you're forced to use a substitute. Other reasons for using substitutes include:

- The manufacturer of the equipment or their local distributor wont sell the part to you (which is actually against the law but some try anyway).
- The part can be purchased but it'll take too long for it to be delivered.
- The part can be purchased but it's too expensive for what it is.
- You'll not be able to charge much for the repair so spending any time tracking the correct transistor down is uneconomical.

When one of these situations applies, the faulty transistor can be replaced with an appropriate substitute. You can work this out for yourself but that takes experience. Instead, you can refer to online transistor cross-references and there are a few (with varying degrees of completeness). Online forums can be useful for this purpose too. However, care must be taken when using transistor cross-references and you should double-check for yourself by comparing data sheets.

Replacing a faulty transistor with a substitute identified by comparing data
If you repair electronics equipment to component level for long enough, one day you'll need to identify a substitute for a faulty transistor that is not listed in a transistor cross-reference. When this happens you'll need to obtain the data for the faulty transistor then compare it to the data of other transistors. Aspects of the faulty transistor and its substitute that should be matched include:

1. Type (that is, NPN or PNP)

   A PNP BJT cannot be substituted for an NPN BJT and vice versa. The biasing conditions for each are opposite in polarity. (Having said that, it can be argued that circuit modifications could allow this type of device substitution but this is beyond the scope of this subject.)

2. Semiconductor (eg silicon, germanium, or silicon-germanium)

   Considering the semiconductor material used for the transistor is most likely to be an issue when repairing older electronics equipment because silicon transistors have been preferred for over well over 30 years now. In fact, it can be difficult to buy germanium transistors from mainstream component suppliers but they're still available from eBay traders.

   That said, some modern RF communications equipment use silicon-germanium BJTs and so the issue of the material used still has relevance today in some specialised applications. Silicon-germanium BJTs for RF applications are readily available from mainstream component suppliers.

   Generally speaking, silicon BJTs are unlikely to be suitable as a straight substitute for germanium BJTs and vice versa. Silicon BJTs have a base-emitter forward voltage drop of ±0.6V whereas it is only ±0.3V for germanium BJTs. So, swapping one for another would upset the quiescent DC biasing conditions around the circuit.

   However, if you have no choice, then one may be substituted for the other and any problems with the quiescent DC conditions may be remedied by minor adjustments to the value of the biasing resistors (preferably in the base circuit).

3. Key electrical specifications

The key electrical specifications that should be compared include:

a) the maximum allowable collector-emitter voltage ($V_{CE(max)}$);
b) the maximum allowable collector current ($I_{C(max)}$);
c) the maximum power dissipation ($P_{(max)}$); and
d) the maximum allowable collector-base voltage ($V_{CB(max)}$).

All transistors have specifications that state the maximum allowable quantity for many of their electrical properties. The most important ones have been listed above (they're also given for a variety of devices in Table 1 on page 5-14). It is not possible to prioritise the specifications above because if any of them is exceeded the BJT will be damaged (if not immediately then over time). When choosing a substitute BJT it's wise to ensure that it has a specification for these electrical properties that is equal to or better than the device that you're replacing. If this proves difficult, choose a substitute with electrical properties equal to or better than the worst the device will experience in circuit.

4. Package (or case)

You might be tempted to think that the type of package that the transistor is in (eg TO-92 or TO-220, etc) should rate higher in importance - obviously it would be silly to replace a transistor in a large package (such as TO-3) with one in a small package (such as TO-92). However, physical size is a function of the transistor's power handling capabilities and this issue should have already been dealt with when comparing the electrical capabilities (see the previous item).

So, the substitute transistor's package only really affects the practical issue of the physical mounting of the transistor. If there are several transistors that are a suitable substitute for the one you're replacing then choose the one that will fit on the heatsink or circuit board with the least need to make modifications to the mounting.

5. Pinout (or lead configuration)

Although the size and shape of many transistor packages are the same or similar, this doesn't necessarily mean that the pinout (that is, which lead is the collector, emitter and base) is the same. In fact, the TO-92 package has three variations with the difference between them only being the pinout.

If you have several transistors that are a suitable substitute for the one you're replacing then choose the one that has the same pinout. If none of them have the same pinout then simply bend the transistor's leads around so that they get soldered on to the correct place on the PCB. However, it is good practice to insulate any of the BJT's leads that cross with a product like *heatshrink*.

6. Beta

   You might be surprised by the fact that the BJT's beta doesn't rate higher as an issue when choosing suitable replacements. But remember that most BJT amplifier circuits use negative feedback to make them fairly independent of beta.

   That being the case, if you're substituting a small signal BJT with another small signal BJT then it is likely to have a beta good enough for the job. This is probably true for power transistors too but it's worthwhile checking that the beta specifications to be sure.

7. Switching speed or maximum operating frequency (F_T)

   The switching speed of most BJTs is high enough to not worry about this specification for most audio applications. However, it becomes critical when repairing high frequency equipment like UHF transmitters and receivers and high frequency switching equipment like switched-mode power supplies. When repairing this type of equipment, ensure that the substitute has a specification for F_T that is equal to or better than the device that you're replacing.

8. Whether the transistor is one of a matched-pair

   Special applications (such as discrete component differential amplifiers) require two transistors known as a *matched pair*. Such transistors have been tested by the manufacturer and are identical in many of their electrical properties, especially the beta (for BJTs). That being the case, if one transistor in a matched pair is damaged then both will need to be replaced.

Using this information and the specifications in Table 1, we can see that a BC549 can be substituted for a BC548 because they are identical in most specifications (though, in some situations, the reverse may not be true). We can also see that an MJ15003 can be substituted for a 2N3055 because, where the specifications are different, the MJ15003 are higher. However, a BD139 cannot be substituted for a BD469 because the BD139's maximum collector voltage rating is far too low.

Choosing a suitable substitute is a little trickier if you don't have data for the faulty BJT. However, the schematic diagram is a big help. It will indicate whether the BJT is NPN or PNP. It'll also indicate the size of the BJT's power supply (*Vcc*). In which case, the substitute should have a rated $V_{CE(max)}$ that is at least the same as the *Vcc*. In most cases, this is a handy rule to apply to the substitute's rated $V_{CB(max)}$ as well.

You can also use the schematic diagram to calculate the transistor's quiescent collector current then choose a substitute with a rated $I_{C(max)}$ that is higher than it. Alternatively, if the BJT is in a power amplifier capable of supplying a known current to a speaker then the substitute must have an $I_{C(max)}$ that is at least this value.

Student notes

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Skill practice 5A

Practise trouble-shooting BJT amplifiers using a DMM

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 75 minutes to complete this exercise.

Equipment

- BJT amplifier fault-finding panel
- digital multimeter
- assorted pin-to-pin leads
- banana leads

Remember:

Follow TAFE NSW WHS guidance at all times!

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Work tasks

1. Read your WHS responsibilities at the top of the form below. Then conduct a WHS risk assessment and record your findings in the space provided.

Responsibilities of students under the Model WHS Act: s28

- Take reasonable care for your own health and safety by working safely at all times
- Take reasonable care to ensure that your acts or omissions don't put the health and safety of others at risk
- Follow all TAFE NSW WHS guidance and comply with all reasonable instructions from TAFE NSW staff to assist them in complying with the TAFE NSW WHS requirements
- In addition to the above, you must:
  - use and maintain machinery, tools and all other equipment properly and safely
  - ensure that your work area is free of hazards
  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

Risks involved in this activity include:	**Control measures:**
Trip hazards (eg students bags) Objects dropped on feet (while equipment is taken to and from workbenches).	Move bags and other objects from walkways Plan lifting of equipment
Others: _____	Other: _____
_____	_____
_____	_____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

3. Use the pin-to-pin leads to set up the cascaded amplifier of Figure 1 on the panel.

   Note 1: Most of the connections have already been made for you. You only need to make the two connections that are shown as thick lines.

   Note 2: There normally wouldn't be a diode on the circuit's *Vcc* rail like this (see top right of the drawing). It's only used on this panel to protect the transistors in case the power supply is accidently connected the wrong way around.

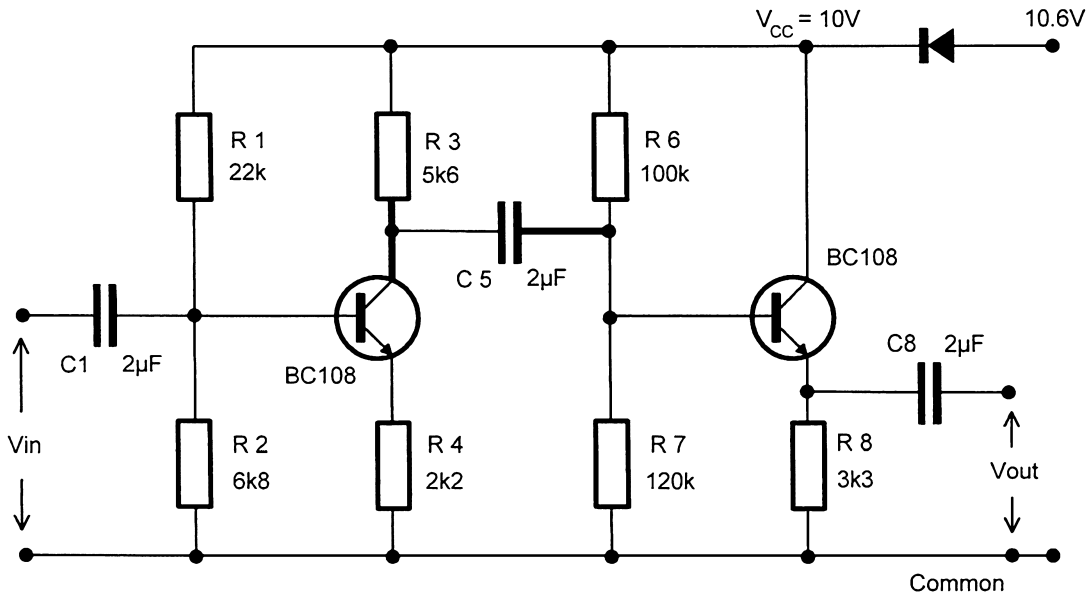

Figure 1

4. Adjust one of the outputs of the bench-mounted DC power supply to 10.6V then turn the supply off.

5. Use banana plug leads to connect the power supply's positive (red) terminal to the panel's *Vcc* line and the negative (black) terminal to the common line.

   Note: The forward voltage drop across the diode is about 0.6V and so this means that the circuit's *Vcc* is 10V not 10.6V.

6. Check that all the fault switches are **OFF** (that is, they're in the up position).

7. Turn the power supply back on.

8. Measure the quiescent DC voltage at the base, emitter and collector of both transistors using the DMM. Record these voltages in the spaces provided on Figure 2 below.

Note: All measurements are with respect to common (in other words, all measurements are made with the meter's black probe must be connected to common)

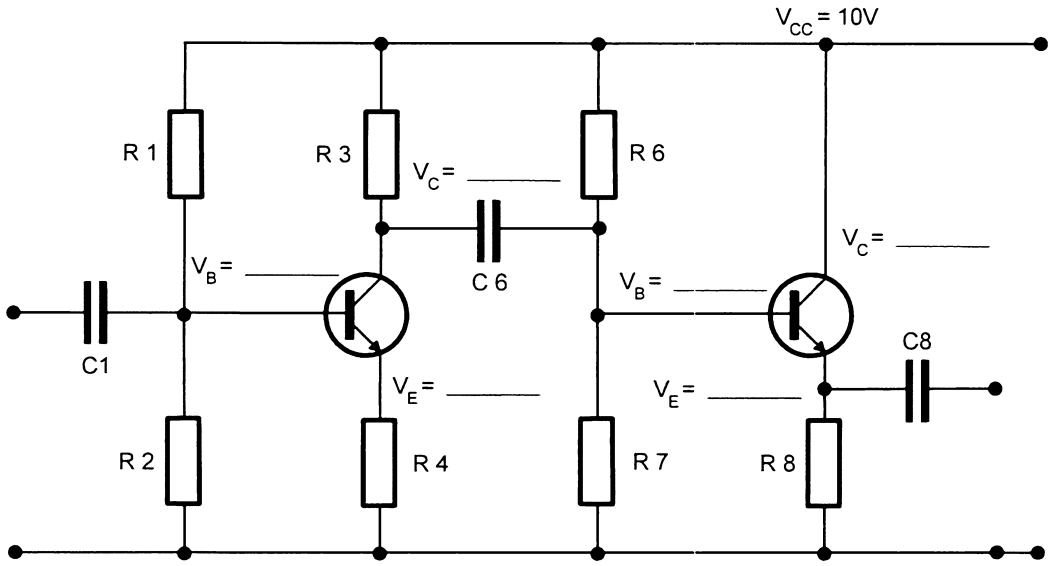

Figure 2

The teacher needs to check your work at this point...

9. Turn on Fault 1.

10. Measure and record the quiescent DC voltages around the BJT shown in Figure 3.

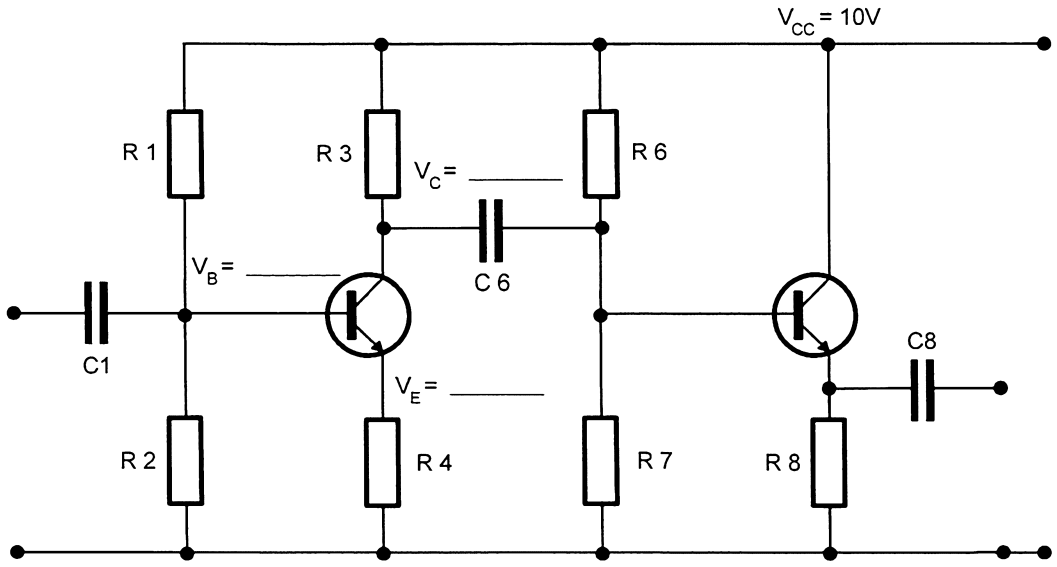

Figure 3

Question 1
What fault is being simulated? Specifiy the number of the component that you think is faulty and what you think is wrong with it.

_____

_____

_____

The teacher needs to check your work at this point...

11. Turn off Fault 1 and turn on Fault 2.

12. Measure and record the quiescent DC voltages around the BJT shown in Figure 4.

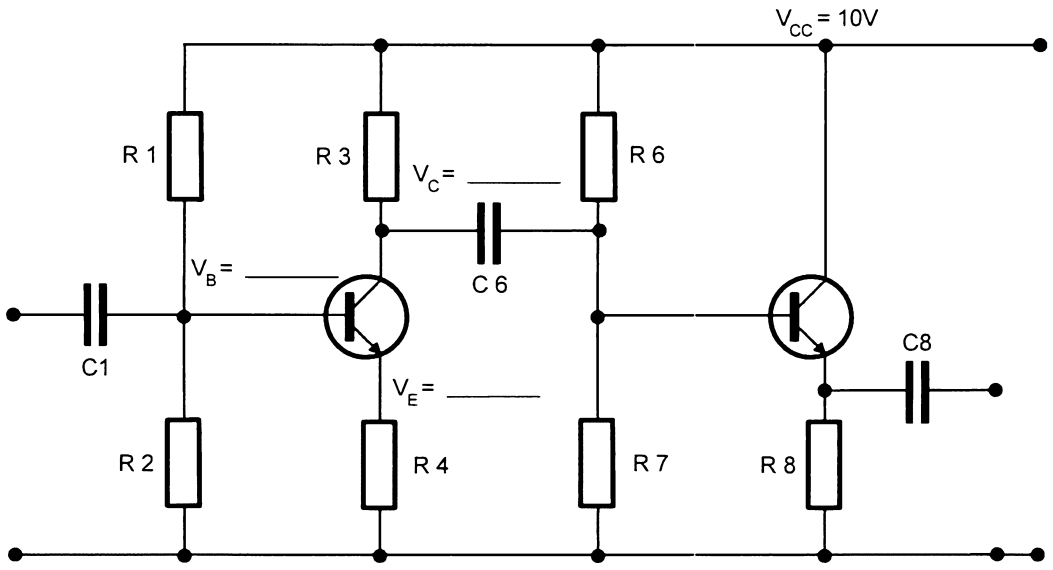

Figure 4

Question 2
What fault is being simulated? Specifiy the number of the component that you think is faulty and what you think is wrong with it.

_____

_____

_____

The teacher needs to check your work at this point...

13. Turn off Fault 2 and turn on Fault 3.

14. Measure and record the quiescent DC voltages around the BJT shown in Figure 5.

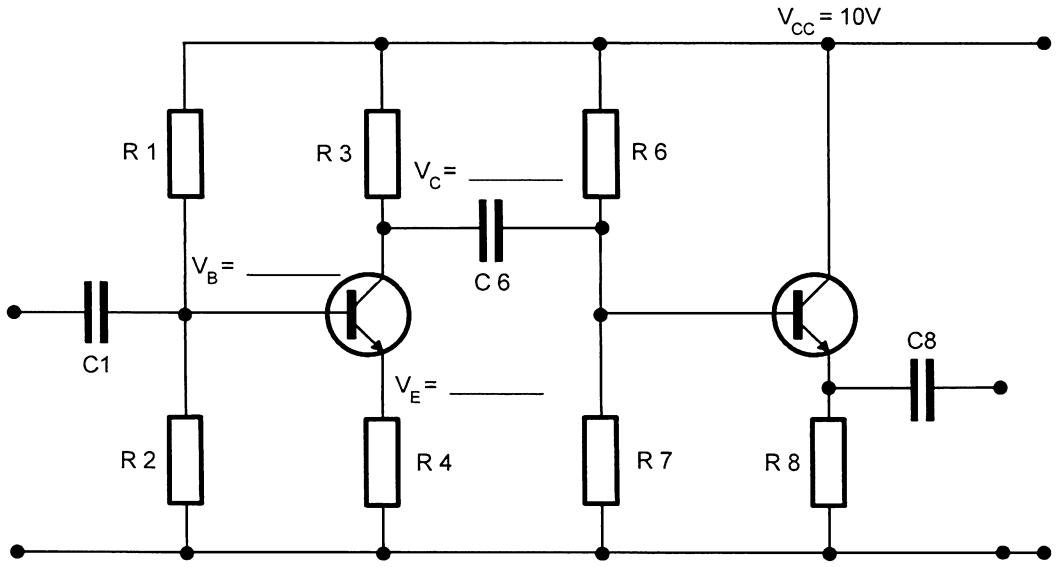

Figure 5

Question 3

What fault is being simulated? Specifiy the number of the component that you think is faulty and what you think is wrong with it.

_____

_____

_____

The teacher needs to check your work at this point...

15. Turn off Fault 3 and turn on Fault 4.

16. Measure and record the quiescent DC voltages around the BJT shown in Figure 6.

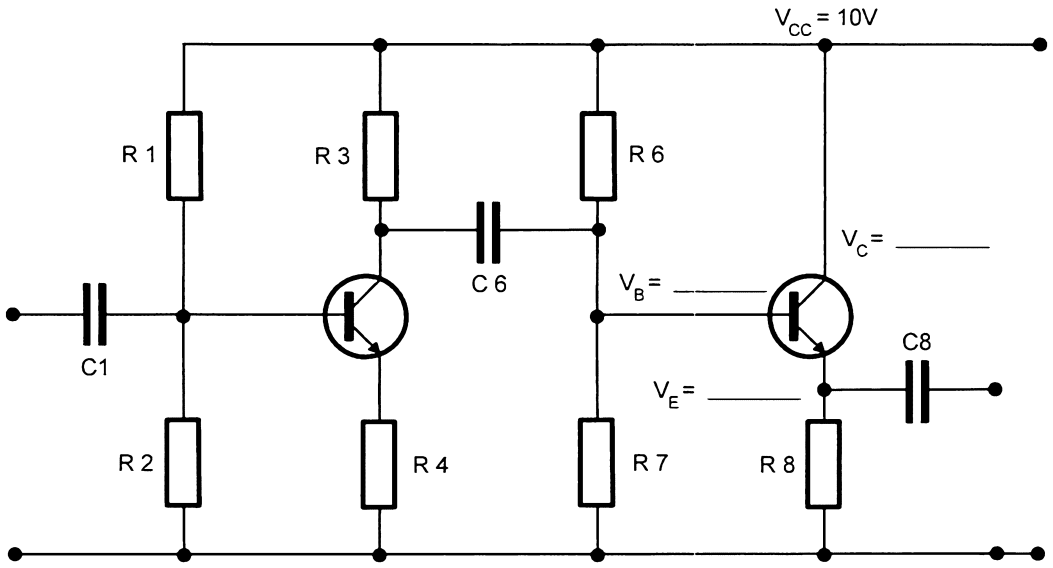

Figure 6

Question 4
What fault is being simulated? Specifiy the number of the component that you think is faulty and what you think is wrong with it.

_____

_____

_____

The teacher needs to check your work at this point...

17. Turn off Fault 4 and turn on Fault 5.

18. Measure and record the quiescent DC voltages around the BJT shown in Figure 7.

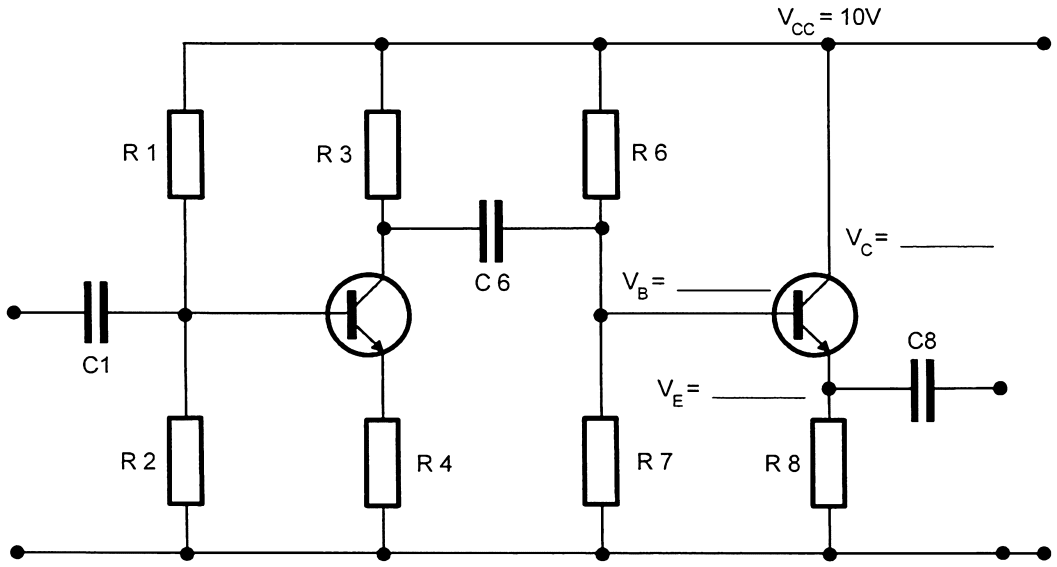

Figure 7

Question 5

What fault is being simulated? Specifiy the number of the component that you think is faulty and what you think is wrong with it.

_____

_____

_____

The teacher needs to check your work at this point...

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Student notes

Skill practice 5B

Testing transistors using the diode test mode of a DMM

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 30 minutes to complete this exercise.

Equipment

- digital multimeter
- 1N4001 diode
- seven assorted transistors (from the teacher)

Remember:

Follow TAFE NSW WHS guidance at all times!

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Work tasks

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  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

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Others: _____	Other: _____
_____	_____
_____	_____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

   Note: The teacher will give you seven transistors some of which could be faulty.

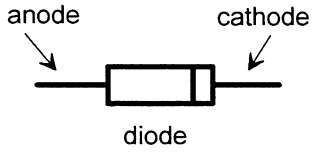
3. Set your multimeter to diode testing (this is usually marked with a diode symbol).

4. Connect the meter leads across the diode so the meter shows a voltage between about 0.55V and 0.75V (that is, the voltage across a forward biased p-n junction).

5. Record which of the meter's leads (red or black) is connected to the diode's **anode** (the p-type material) when the meter shows this voltage.

Table 1

Which lead is connected to the anode: RED or BLACK?	



6. Take one of the transistors and identify its part number. Record this in Table 2 (on the next page).

7. Sketch the transistor's package in the next column along.

8. Use your mobile phone or one of the classroom's desktop computers to obtain the datasheet for the transistor.

9. Use the datasheet to identify the transistor's pins and show these on your sketch.

10. Use the datasheet to identify whether the transistor is an NPN or PNP type and record this in the next column along.

11. Test the transistor and identify whether or not it's faulty.

    Note: One or more of the transistors may be faulty.

12. Repeat Steps 6 to 11 for the remaining six transistors.

    Note: Check with the teacher occasionally to make sure you're on the right track.

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Table 2

Transistor part number	Sketch of lead configuration	NPN or PNP?	Working? Yes/No

The teacher needs to check your work at this point...

Review questions

Answer these questions to check your understanding of what you have learnt for this chapter. Doing this will also help to prepare you for the tests.

1. List five effects on an AC signal at the output of a BJT amplifier circuit that would indicate that it is faulty.

2. Why is it a **bad** idea to simply remove and test all the components in a faulty circuit?

3. You've compared the input and output signals of a BJT amplifier circuit and suspect that it is faulty. What is the **first** measurement that you should perform?

4. Explain why the circuit's *Vcc* is the most important first measurement.

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Question 5 refers to the circuit in Figure 1 below

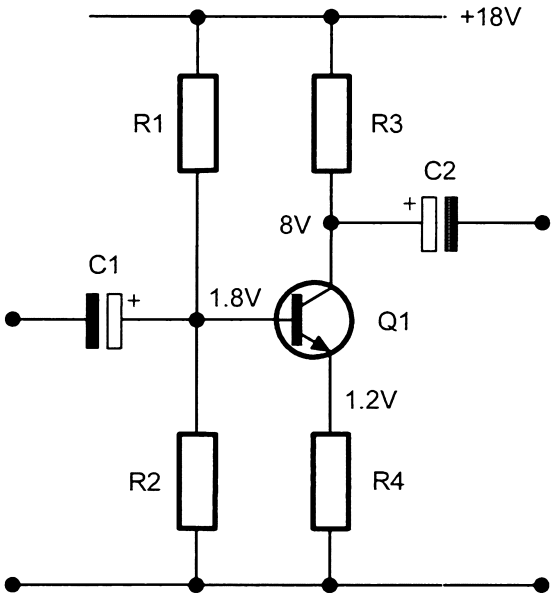

Figure 1

5. Figure 1 above shows a voltage divider biased NPN BJT circuit and its normal quiescent DC voltages. Table 1 below lists the voltages measured around the circuit for seven faults. Use this information to determine the likely cause of each fault.

Table 1

	V_B	V_E	V_C	Cause
i)	6V	5.4V	6.7V	
ii)	1.8V	1.2V	14V	
iii)	0.9V	0.9V	18V	
iv)	1.8V	1.2V	18V	
v)	1.8V	1.2V	0V	
vi)	0V	0V	18V	
vii)	1.8V	5V	5V	

6. List at least five things to consider when choosing a replacement transistor.

7. Explain how you use a digital multimeter to find out whether it is an NPN or PNP type.

8. State whether the following transistor substitutes are ok or not, and give a reason why. Use the data on page 5-2 to inform your decision.

   (a) BC549 replaced with BC559 _____

   (b) BC548 replaced with MJ15003 _____

   (c) BD640 replaced with BD140 _____

   (d) BC548 replaced with BC549 _____

   (e) MJE3055 replaced with 2N3055 _____

   (f) BF180 replaced with BC337 _____

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Student notes

Section 6 Junction field effect transistors

Purpose To develop your understanding of the principles of operation and biasing methods of junction field effect transistors to help you locate amplifier faults by comparing predicted and measured DC voltages around two common JFET biasing circuits.

Objectives At the end of this section you should be able to:

- Draw and identify the schematic symbols for N-channel and P-channel JFETs
- Name the three terminals of a JFET
- Describe the bias conditions needed for each junction of a JFET for it to operate in amplifier circuits
- Show the direction of current flow and voltage polarity at each terminal of the JFET
- Explain the operating principles of JFETs
- Interpret graphs for JFET input-output transfer characteristics
- Identify typical biasing circuits used for N-channel and P-channel JFETs
- Explain the function of each component in the self bias and voltage divider bias JFET circuits
- Calculate the voltages around self biased and voltage divider biased JFET circuits
- Verify the relationship between gate-source voltage and drain-source current of a JFET

Introduction

Field Effect Transistors or FETs are amplifying devices like BJTs. Their construction and principle of operation are different to BJTs but many of the ideas about biasing and amplifier configurations are the same. There are several different types of FET and in this section you'll learn about the Junction Field Effect Transistor or JFET.

Junction field effect transistors (JFETs)

When compared to BJTs, JFETs have the following advantages and disadvantages:

Advantages

- Higher input resistance (typically more than 100MΩ)
- No thermal runaway problems (conduction does not increase with heat)
- Less introduced noise

Disadvantages

- Lower gain
- Lower bandwidth (not as good at amplifying high frequencies)

N-channel and P-channel JFETs

There are two types of JFET, N-channel and P-channel, which can be compared with NPN and PNP BJTs respectively. Their schematic symbols and representative physical construction are shown in Figures 1 and 2. The three terminals of a JFET are called drain, gate and source and can be compared to the collector, base and emitter of a BJT respectively.

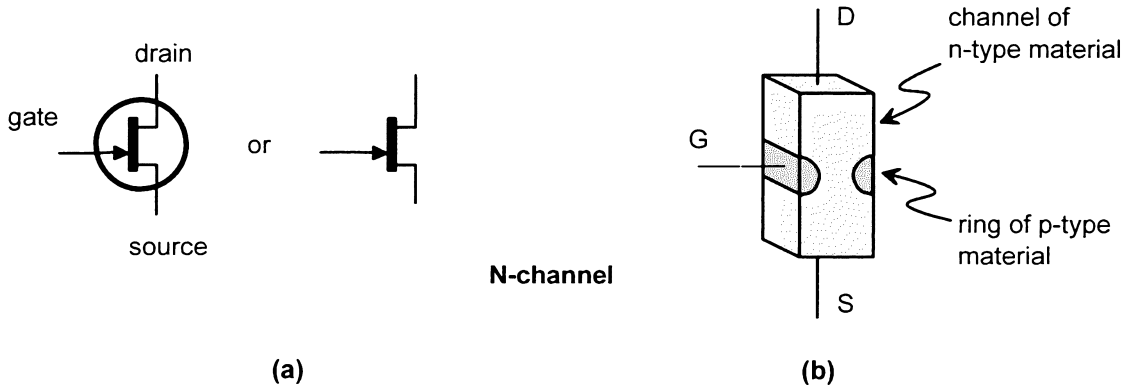

Figure 1 *(a) Schematic symbol of an N-channel JFET; and (b) cross-sectional view of JFET construction*

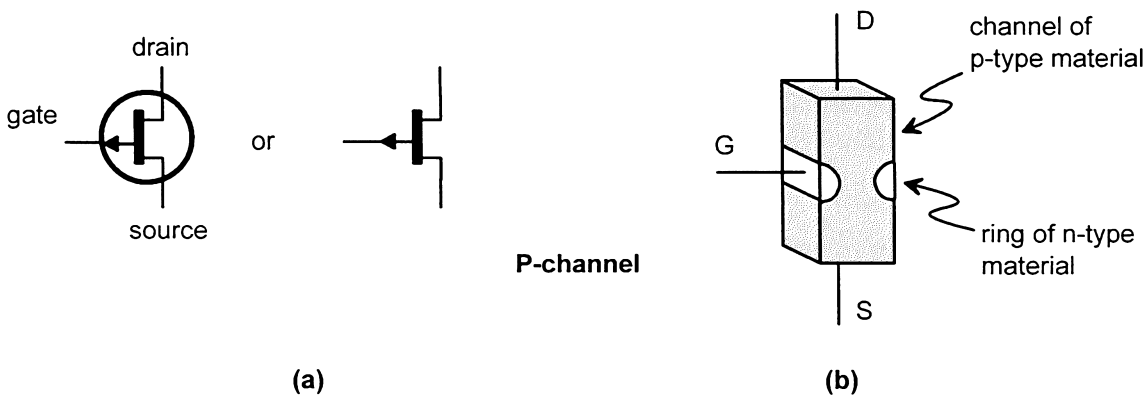

Figure 2 *(a) Schematic symbol of a P-channel JFET; and (b) cross-sectional view of JFET construction*

Figures 1a and 2a show the schematic symbols used for an N-channel and P-channel JFET respectively. There are three things you should notice about the symbols:

- The gate is the middle leg
- The gate is shown slightly off-centre and is closer to the source
- The arrow points into the gate for an N-channel JFET
- The arrow points out of the gate for a P-channel JFET

Figures 1b and 2b show the approximate construction of the two types of JFET. These diagrams help explain how each device gets its name. The N-channel JFET has a piece of n-type doped silicon connected to both the drain and source acting as a channel for current to flow through. The P-channel JFET has exactly the same construction with the channel being made from p-type material.

As the drain-source region is one piece of semiconductor material, the drain-source connection acts like a resistor. However, we can still think of the gate-drain and gate-source connections as p-n junctions.

Testing JFETs using a digital multimeter

Like BJTs, JFETs can be tested using a digital multimeter. In fact, the gate-source and gate-drain connections are tested in exactly the same way as the base-emitter and base-collector connections of a BJT because they form p-n junctions.

The only difference between the JFET and the BJT is the readings you get when testing between the drain and source terminals. Recall that a BJT reads "OL" between the collector-emitter connections (in either polarity) but the JFET reads a resistance from a few hundred ohms up to a couple of kilo ohms (depending on the type of device) between the drain-source connections (in either polarity).

JFET operation

It is useful to describe the JFET's operation by comparing it to the operation of a BJT. You may remember that a BJT is a *current-controlled* device. The collector-emitter connection is an open-circuit unless a potential difference across the base and emitter forward biases the base-emitter p-n junction. When this happens, a base current flows which causes a collector current to flow that is larger than the base current by a factor of beta.

Although the JFET is a transistor, it is different to the BJT in two very important ways. First, the JFET's drain-source connection is not an open-circuit. It is more like a resistor which means that, if a power supply is connected between the drain and source, a drain-source current (I_{DS}) flows even if the gate-source voltage (V_{GS}) is zero volts. This is shown for both an N-channel and a P-channel JFET in Figure 3 below.

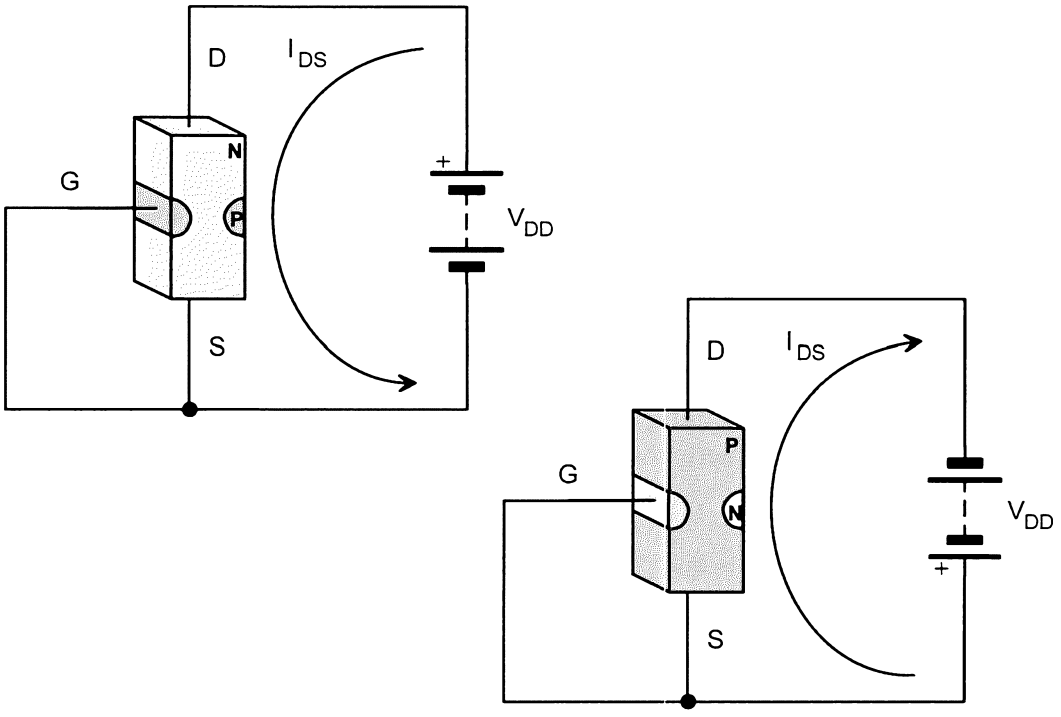

Figure 3 *A drain-source (conventional) current flows even if the gate-source voltage is zero*

The second way in which the JFET is different to the BJT involves the polarity of the biasing voltage on the gate relative to the voltage on the source and the voltage on the drain.

Recall that, for a BJT, the polarity of the base voltage is set so that the p-n junction formed by the base-emitter connection is forward biased but the p-n junction formed by the base-collector connection is reverse biased. With JFETs, the polarity of the gate voltage is set so that the both p-n junctions formed by the gate-source and gate-drain connections are reverse biased. This is shown for both an N-channel and a P-channel JFET in Figure 4 below.

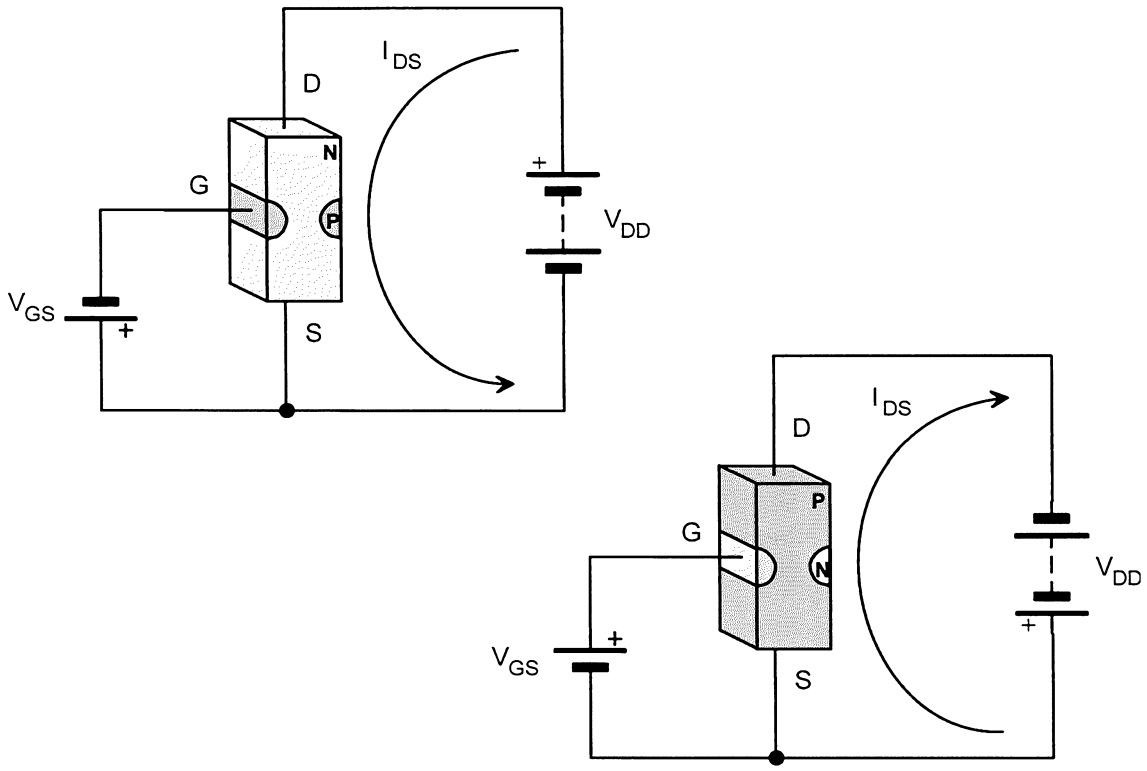

Figure 4 *The gate voltage is set so that the p-n junctions formed by the gate-source and gate-drain connections are reverse biased*

Importantly, with both the gate-source and gate-drain junctions reverse biased there is no current flowing either in or out of the JFET's gate (other than a minute amount of *leakage current* which we can ignore).

So, how does the JFET work? To answer this question, you need to know a little more about p-n junction action. Recall that whenever n-type and p-type semiconductors come into contact, free electrons match-up with spaces for electrons (called *holes*) in a small region either side of the junction. As a result, there are fewer free *current carriers* (electrons and holes) in this region and this reduces the junction's ability to conduct current. Recall that the name given to this region is the *depletion layer* and it is shown in Figure 5 below.

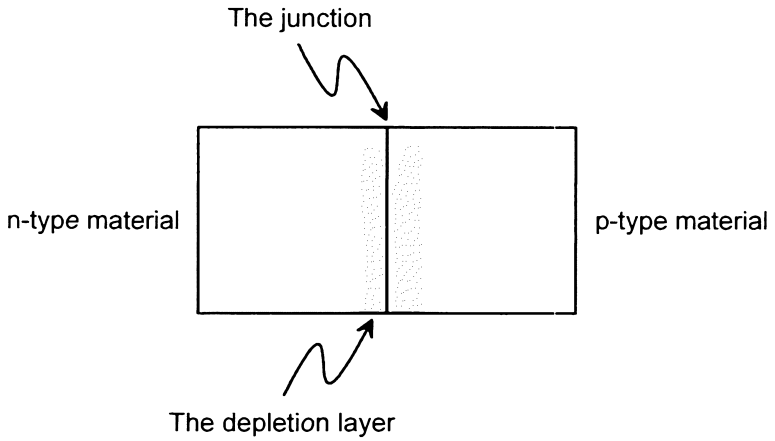

Figure 5 *The depletion layer on either side of a p-n junction*

As you know, connecting an EMF across the junction in the correct polarity can effectively reduce the depletion layer as shown in Figure 6 below. (And, as you also know, once the EMF's potential difference is 0.6V, the depletion layer is effectively reduced to nothing and current readily flows through the junction.)

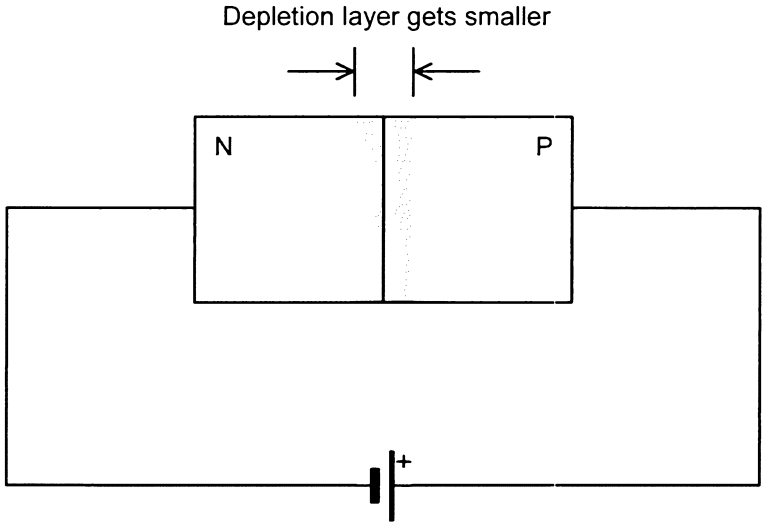

Figure 6 *Making the p-type material positive with respect to the n-type material makes the depletion layer smaller*

However, you may not know that the reverse is also true. Connecting an EMF across the junction in the "wrong" polarity can effectively increase the depletion layer's size as shown in Figure 7 below.

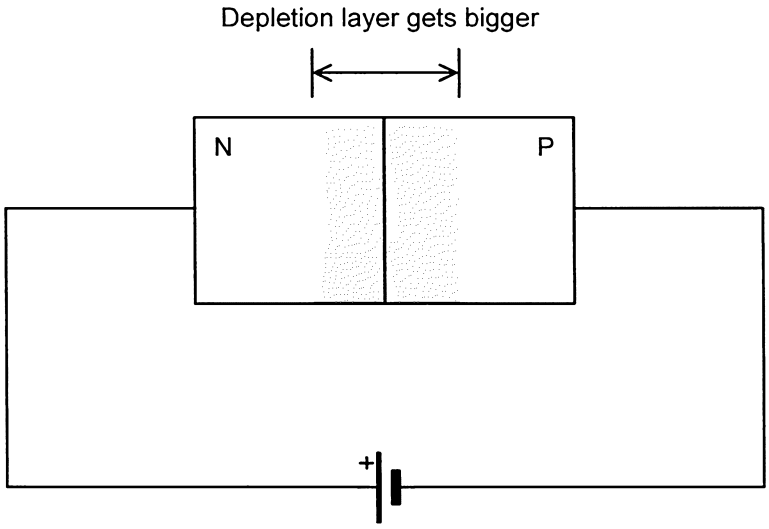

Figure 7 *Making the n-type material positive with respect to the p-type material makes the depletion layer bigger*

Note: Saying that the depletion layer gets smaller or bigger is a bit of an oversimplification but a useful one for our purposes here. For an excellent, easy to read explanation of p-n junction action, read the first chapter of *Electronics Devices* by Thomas Floyd (which is available in the College's library).

Lets now return to the operation of a JFET. As the p-type and n-type semiconductor materials are touching, a depletion layer develops inside the channel around the ring of material that the gate terminal is connected to (see Figure 8 below).

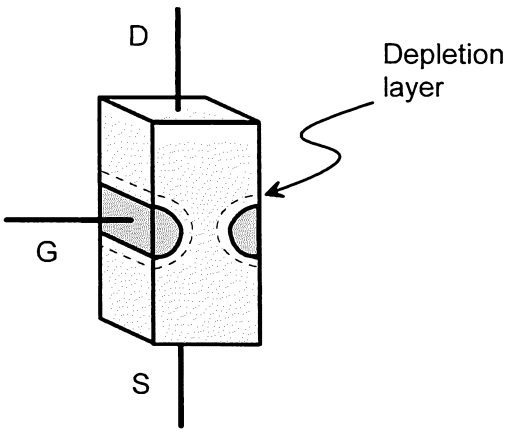

Figure 8 *A depletion layer develops inside the channel of a JFET*

As the depletion layer is a region of low conductivity, it effectively "squeezes" the channel a little in the middle and helps to set the channel's "natural" resistance.

Following the previous discussion of p-n junction action, it's clear that if the polarity of the JFET's gate-source voltage is such that it reverse biases the JFET's p-n junction, the depletion layer gets bigger as shown in Figure 9 below using an N-channel JFET.

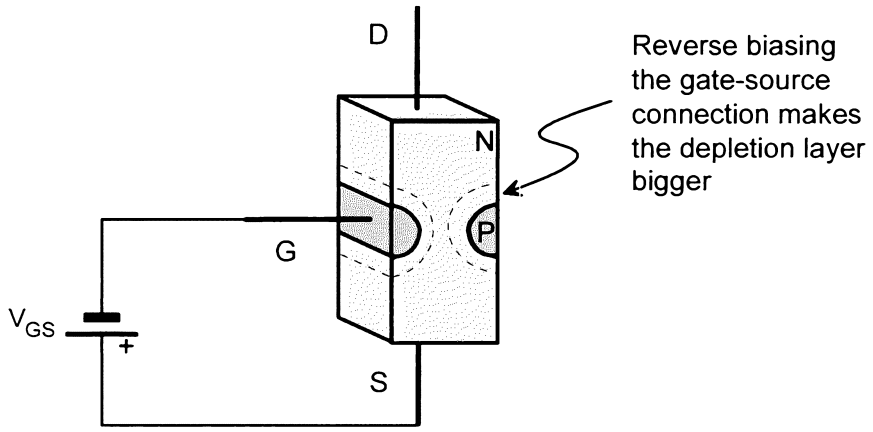

Figure 9 *By reverse biasing the gate, the depletion layer can be made bigger*

Importantly, the increase in the depletion layer "squeezes" the channel more and reduces its ability to conduct current. In other words, the drain-source current goes down. And, if the p-n junction is sufficiently reverse biased, the channel can be choked-off altogether and no drain-source current flows.

Notice from this explanation that it's the JFET's gate voltage that influences how much drain-source current that flows. That's why JFETs (and MOSFETs too) are often said to be "current-controlled" devices.

The V_{GS}-I_{DS} transfer characteristic

The operation of a JFET can be described using a graph which might make it more meaningful to you. Figure 10 below shows the graph of gate-source voltage versus drain-source current for an N-channel JFET.

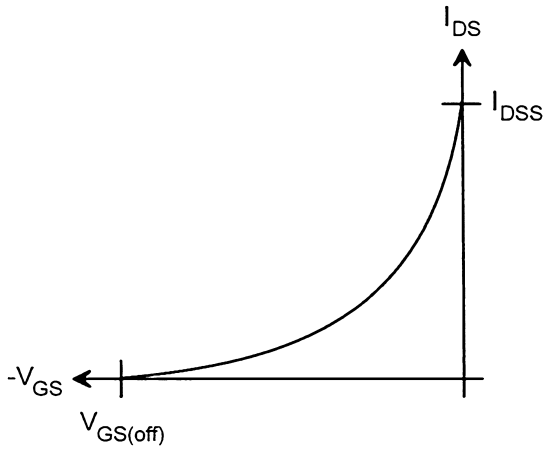

Figure 10 *The graph of V_{GS} versus I_{DS} for an N-channel JFET*

The graph shows that the drain-source current is at maximum when the gate-source voltage is zero. This current is known as the *saturation* drain-source current (I_{DSS}). As the gate voltage is made increasingly negative relative to the source, the drain-source current goes down (because the depletion layer gets thicker). And, if the gate voltage is made negative enough, the drain-source current drops to zero (because the depletion layer has gotten so thick that it has choked-off the channel). This voltage is known as $V_{GS(off)}$ and ranges from -2V to -8V depending on the type of JFET.

Figure 11 below shows the graph of gate-source voltage versus drain-source current for a P-channel JFET. As you can see, the principle of operation is the same but the polarity of gate-source voltage and direction of drain-source current are opposite.

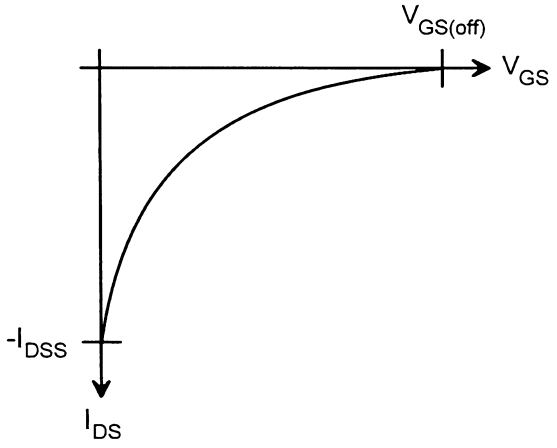

Figure 11 *The graph of V_{GS} versus I_{DS} for a P-channel JFET*

JFET biasing circuits

There are two main JFET biasing circuits: (1) Self bias; and (2) Voltage divider bias.

Self bias

Figure 12 shows the circuit of a self biased JFET amplifier. This is the most common JFET biasing method.

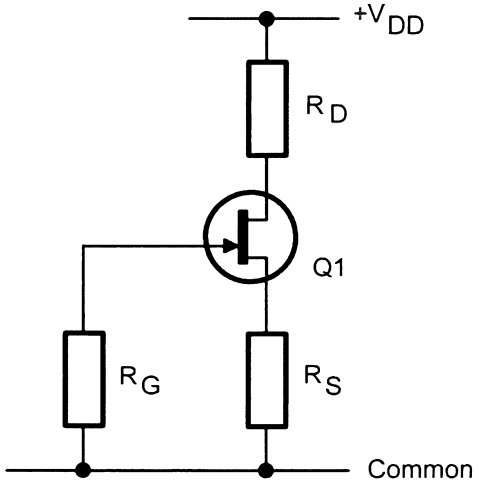

Figure 12 *The self bias N-channel JFET amplifier*

How the biasing works

From the discussion so far, the biasing of an N-channel JFET requires the gate be made negative with respect to the source. But as you can see from the diagram in Figure 12 a negative power supply isn't used. So how does self bias work? The answer is simple. Instead of making the gate negative with respect to the source, the self bias circuit makes the source positive with respect to the gate which is the same thing!

To understand how this happens let's start with the gate circuit. As you can see, the JFET's gate is connected to ground by R_G. As no current flows in or out of a JFET's gate, there is no current through R_G. This means that R_G has no potential difference across it and so the voltage on the JFET's gate is the same as the voltage of the common rail. In this condition, the gate is said to be "pulled down" to 0V.

Recall from the earlier discussion of JFET operation that even with zero volts on the gate, there can still be a drain-source current (I_{DS}). This current develops a potential difference across the source resistor (R_S) making the JFET's source positive with respect to common and hence more positive than the gate. In the process, V_{GS} is negative and the circuit has set up its own bias.

To prove that V_{GS} is negative under these conditions, Figure 13 shows the JFET with 0V on its gate (as you would expect to have with the self bias circuit) and +2V on its source (which is typical). As the meter shows, V_{GS} is -2V.

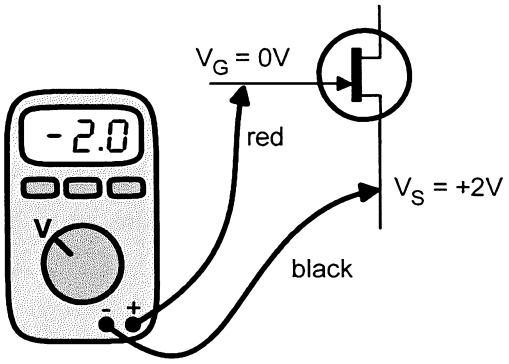

Figure 13 *The gate can be made negative with respect to the source by making the source positive with respect to the gate*

The function of each component in the circuit is as follows:

- The power supply (V_{DD}) provides DC power to the circuit and provides the biasing voltages for the drain and source.
- The gate resistor (R_G) clamps the gate to zero volts.
- The transistor (Q_1) converts variations in gate voltage to variations in drain-source current.
- The source resistor (R_S) sets the drain-source current and the source voltage (V_S).
- The drain resistor (R_D) provides a path for the drain current to flow. It also sets up the quiescent DC drain voltage (V_D) and converts changes in drain-source current to changes in drain voltage.

Calculating the quiescent DC voltages around the self bias circuit

Recall that one of the ways that technicians can check the operation of BJT amplifiers is to measure the quiescent DC voltages around the circuit (with respect to common) then compare them to what they should be. If they're about the same then the circuit is probably working correctly. But if not then there may be a problem. Not surprisingly, the process is the same for checking FET amplifiers.

Again though, the quiescent DC voltages may not be written on the schematic diagram. That being the case, you need to know how to calculate them. Calculating the gate voltage is simple.

Find V_G — As there is no gate current and the gate is connected directly to ground via a resistor then:

$$V_G = 0V$$

Calculating the theoretical source voltage involves a process that is beyond what is expected of a technician so this is not demonstrated here. Instead, you'll be given a value for the gate-source voltage (V_{GS}) (or a means of working it out logically) which you will use to calculate the source voltage for circuits in this subject.

Find V_S — When you've been given the gate source voltage (V_{GS}) then:

$$V_S = V_G - V_{GS}$$

Calculating the drain voltage is a two-step process that is basically the same as finding the collector voltage in voltage divider BJT amplifier circuits.

1. Find I_{DS} — The drain-source current is found using Ohm's Law:

$$I_{DS} = \frac{V_S}{R_S}$$

2. Find V_{RD} — The potential difference across the drain resistor is found using Ohm's Law:

$$V_{RD} = I_C \times R_D$$

3. Find V_D — The drain voltage is found using Kirchhoff's Voltage Law:

$$V_D = V_{DD} - V_{RD}$$

As with BJTs, you're unlikely to need to measure the drain-gate voltage and the drain-source voltage to locate a fault. However, you may need to calculate these voltages if the circuit uses a JFET that you can no-longer buy and you want to substitute it with a suitable replacement.

Find V_{DG} The voltage at the drain with respect to the gate is found by simply subtracting the gate voltage from the drain voltage.

$$V_{DG} = V_D - V_G$$

Find V_{DS} The voltage at the drain with respect to the source is found by simply subtracting the source voltage from the drain voltage.

$$V_{DS} = V_D - V_S$$

Practise calculating the quiescent DC voltages around a self biased JFET amplifier by trying the following questions.

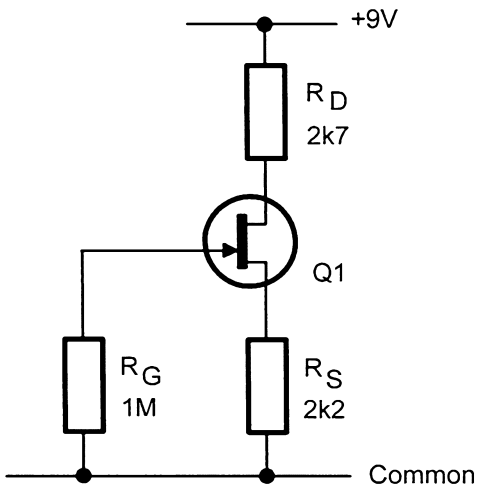

Figure 14

1. What is the gate voltage (V_G) for the circuit in Figure 14?

2. Calculate the source voltage (V_S) if gate-source voltage (V_{GS}) is -2.5V.

3. Calculate the drain-source current (I_{DS}).

4. Calculate the drain voltage (V_D).

5. Calculate the drain-gate voltage (V_{DG}).

6. Calculate the drain-source voltage (V_{DS}).

Voltage divider bias

Figure 15 shows the circuit of the voltage divider biased JFET amplifier.

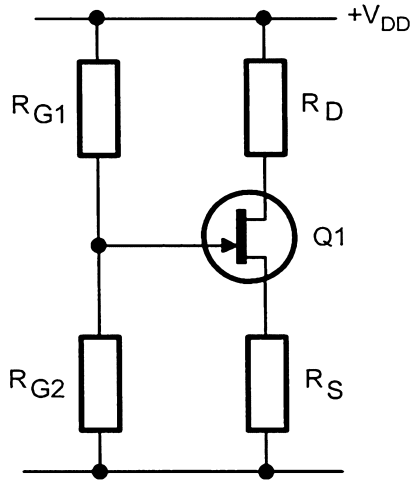

Figure 15 *The voltage divider bias N-channel JFET amplifier*

How the biasing works

The biasing of this circuit is almost identical to that of the self bias. The difference is, the gate is held at a small positive voltage due to the voltage divider set up by R_{G1} and R_{G2}. If the circuit has been designed correctly, the drain-source current develops a potential difference across the source resistor (R_S) that is larger than the positive voltage on the gate, again setting up a negative gate-source voltage.

The function of each component in the circuit is as follows:

- The power supply (V_{DD}) provides DC power to the circuit and provides all the necessary biasing voltages.
- The gate resistors (R_{G1} *and* R_{G2}) set the gate voltage.
- The transistor (Q_1) converts variations in gate-source voltage to variations in drain-source current.
- The source resistor (R_S) sets the drain-source current and the source voltage (V_S).
- The drain resistor (R_D) provides a path for the drain current to flow. It also sets up the quiescent DC drain voltage (V_D) and converts changes in drain-source current to changes in drain voltage.

Calculating the quiescent DC conditions around the voltage divider bias circuit
Except for the gate voltage, the quiescent DC voltages around the circuit can be calculated using exactly the same equations as those for the self bias circuit. The gate voltage is found by using the voltage divider principle (in the same way that the base voltage is found in the voltage divider biased BJT amplifiers).

Find V_G The gate voltage is found using the voltage divider principle (in the same way that the base voltage is found in the voltage divider biased BJT amplifiers).

$$V_G = V_{DD} \times \frac{R_{G2}}{R_{G1}+R_{G2}}$$

Practise calculating the quiescent DC voltages around a voltage divider biased JFET amplifier by trying the following questions.

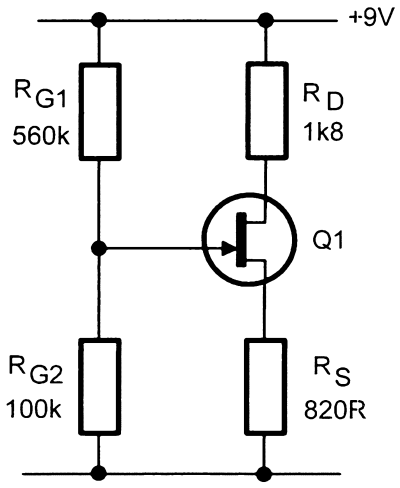

Figure 16

1. Calculate the gate voltage (V_G) for the circuit of Figure 16.

2. Calculate the source voltage (V_S) if the gate-source voltage (V_{GS}) is -1V.

3. Calculate the drain-source current (I_{DS}).

4. Calculate the drain voltage (V_D).

5. Calculate the drain-source voltage (V_{DS}).

The effects of faults on the DC voltages around JFET circuits

Like BJT circuits, most faults in JFET biasing circuits change the DC quiescent voltages around the circuit. With a good understanding of JFET theory and knowledge of how JFETs and other components typically fail, it's usually possible to work out which component is faulty from the voltage measurements that you take.

The following is a list of some of the likely component faults and their effects on the DC quiescent voltage levels around a self biased JFET circuit.

- *Q1* open-circuit drain

  If the JFET's drain is open-circuit, there is no-longer a path for drain-source current to flow. With no drain-source current, there's no potential difference across the drain resistor and so the voltage on the JFET's drain equals the supply voltage and the voltage on the source is 0V. However, the gate voltage is unaffected.

- *Q1* open-circuit source

  This has the same effect as an open-circuit drain for the same reasons.

- *Q1* open-circuit gate

  If the JFET's gate is open-circuit, the gate voltage is unchanged (because the "break" is inside the device). Drain-source current still flows but the amount is no-longer affected by the apparent gate-source voltage. That being the case, the drain and source voltages change. The drain voltage most likely goes down and the source voltage most likely goes up.

- *Q1* short-circuit gate-source

  If the JFET's gate and source terminals are short-circuit the voltage on all the JFET's terminals change. The new voltages are affected by the values of other circuit components and cannot be presumed to move one way or the other. However, the fault is immediately recognisable because the gate voltage is no-longer 0V. Instead it is the same voltage as the source.

- *Q1* short-circuit drain-gate

  If the JFET's gate and drain terminals are short-circuit they'll have the same voltage and it'll probably be similar to (but not the same as) the voltage that is normally on the source. The voltage on the gate is unaffected. The voltage on the drain and source terminals can be easily calculated because the drain and source resistors end up forming a simple voltage divider with this fault.

- R_G high

  If R_G is high the effect depends on how high it has drifted. If only a little, there is no effect because the resistor is only there to clamp the gate to common. However, if R_G has drifted very high then the effect is the same as R_G open-circuit.

- R_G open-circuit

  If R_G is open-circuit, the gate is no-longer 0V. Instead the gate floats around a 100mV or so. This affects the drain and source voltages which float about their normal operating voltages.

- R_S high

  If R_S is high in value, the source voltage is bigger than it should be which means that the gate-source voltage is bigger than it should be. This has two possible effects. First, the drain-source current is smaller and so the drain voltage is bigger than it should be. Alternatively, the value of R_S could drift so high that the effect is the same as it going open-circuit.

- R_S open-circuit

  If R_S is open-circuit, there is no-longer a path for the drain-source current. This means that the voltage on the source floats around 0V and the voltage on the drain equals the supply voltage. The voltage on the gate is unaffected.

- R_D high

  If R_D is high in value, the potential difference across it is greater than normal and so the voltage on the drain is lower than normal. The voltage on the gate and source are unaffected.

- R_D open-circuit

  If R_D is open-circuit there is no-longer a path for the drain-source current to flow. This means that the voltage on the drain and source is 0V. The voltage on the gate is unaffected.

Note: It's probably not worth memorising the effects of these faults. If you have a good understanding of JFET operation and the operation of the biasing circuits, you can work these out with practise.

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Student notes

Skill practice 6

Practise measuring DC voltages and currents in JFET amplifiers using a DMM

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 1¼ hours to complete this exercise.

Equipment

- prototyping panel
- two DMMs (only one set of meter leads is needed)
- decade box
- 2N5485 JFET
- 1MΩ ¼W resistor
- 2k2Ω ¼W resistor
- banana leads
- hook-up wire
- wire strippers

Remember:

Follow TAFE NSW WHS guidance at all times!

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Work tasks

1. Read your WHS responsibilities at the top of the form below. Then conduct a WHS risk assessment and record your findings in the space provided.

Responsibilities of students under the Model WHS Act: s28

- Take reasonable care for your own health and safety by working safely at all times
- Take reasonable care to ensure that your acts or omissions don't put the health and safety of others at risk
- Follow all TAFE NSW WHS guidance and comply with all reasonable instructions from TAFE NSW staff to assist them in complying with the TAFE NSW WHS requirements
- In addition to the above, you must:
  - use and maintain machinery, tools and all other equipment properly and safely
  - ensure that your work area is free of hazards
  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

Risks involved in this activity include:	**Control measures:**
Trip hazards (eg students bags) Objects dropped on feet (while equipment is taken to and from workbenches).	Move bags and other objects from walkways Plan lifting of equipment
Others: _____	Other: _____
_____	_____
_____	_____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

3. Set the left-side output of the bench-mounted DC power supply to 0V and the right-side output to 10V. Then turn off the power supply.

4. Wire the circuit of Figure 1 paying special attention to the polarities of both power supply connections.

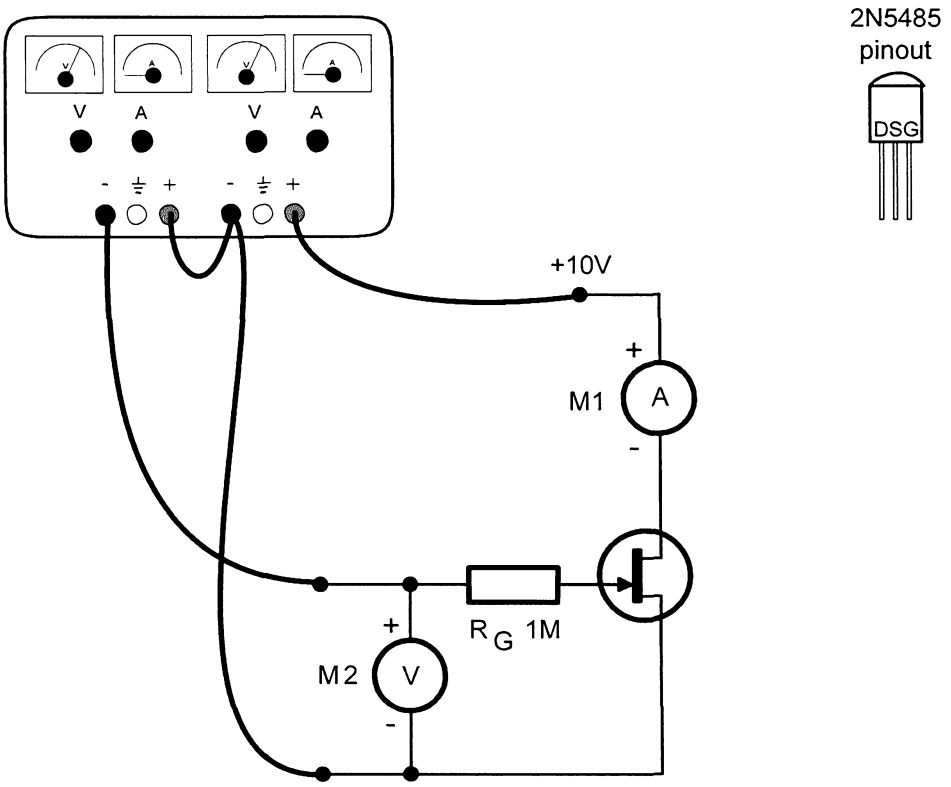


Figure 1

5. Adjust M1 for measuring currents in the mA range.

6. Adjust M2 for measuring DC potential differences (voltages).

7. Turn on the bench-mounted power supply.

8. Measure the drain-source current and record the value in Table 1 in the space for V_{GS} = 0V.

9. Increase the voltage of the left-side power supply output by 0.25V.

10. Measure and record the new drain-source current.

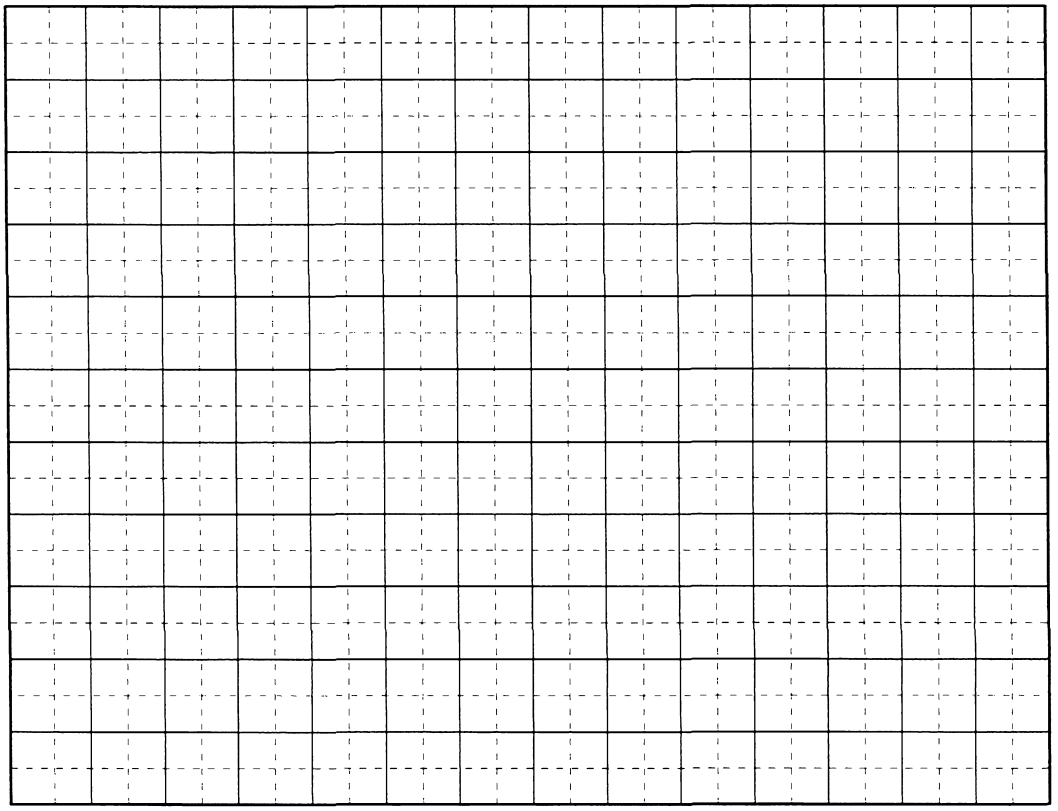
11. Repeat steps 9 and 10 for the remaining gate-source voltages in Table 1.

Table 1

V_{GS}	I_{DS}	V_{GS}	I_{DS}
0		-1.5	
-0.25		-1.75	
-0.5		-2	
-0.75		-2.25	
-1		-2.5	
-1.25		-2.75	

The teacher needs to check your work at this point...

12. Plot the graph of V_{GS} versus I_{DS}. Use the X-axis for V_{GS}.



Question 1
What is the saturated drain-source current (I_{DSS}) of your JFET?

Question 2
What is the approximate $V_{GS(off)}$ voltage of your JFET?

Question 3
Why is the drain-source current maximum when the gate-source voltage (V_{GS}) is 0V?

The teacher needs to check your work at this point...

13. Turn off the power supply.

14. Modify the circuit as shown in Figure 2.

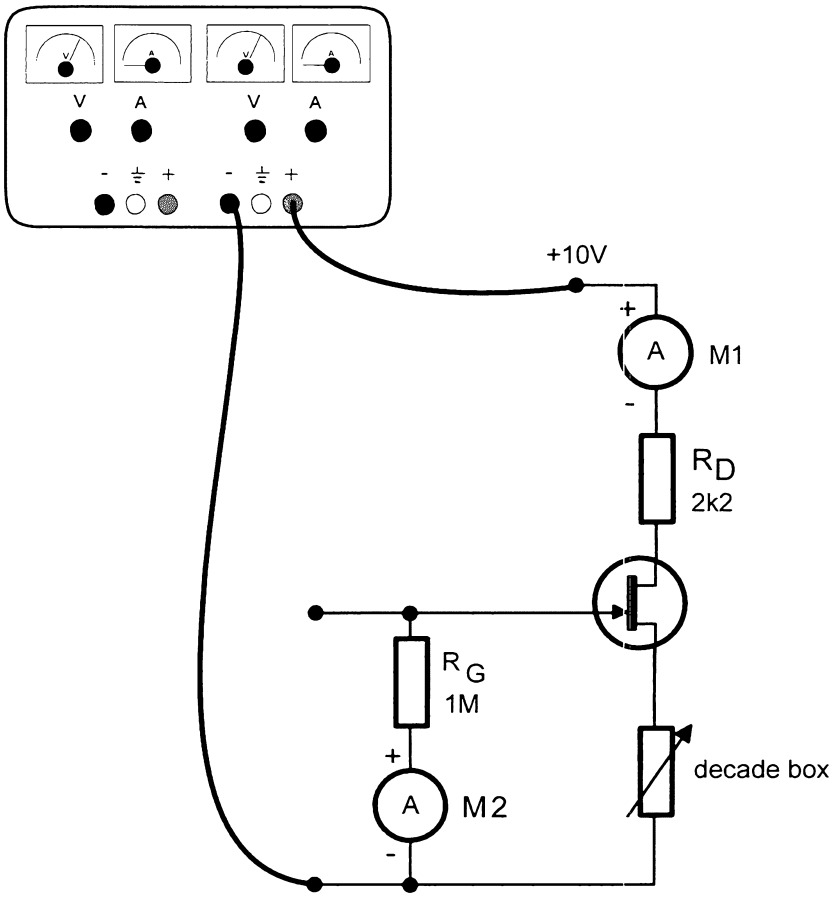


Figure 2

15. Set the decade box to a resistance of 600Ω.

16. Adjust M1 for measuring currents in the mA range and M2 for measuring currents in the μA range.

17. Turn on the power supply.

18. Measure the gate current and the drain-source current. Record your measurements in Table 2.

19. Disconnect M2 and connect R_G directly between the JFET's gate and common.

20. Use the meter to measure and record the drain, source and gate voltages.

Table 2

I_G	
I_{DS}	
V_D	
V_S	
V_G	

21. Calculate V_{GS} using the measured values of V_G and V_S. Record this value in Table 3.

22. Measure and record V_{GS} using the DMM.

Table 3

V_{GS} calculated	V_{GS} measured

Question 4
Why is V_{GS} a negative voltage when the power supply to the circuit is positive?

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Question 5
Why wasn't there any current flowing into the gate?

_____

_____

The teacher needs to check your work at this point...

23. Change the decade box's value (R_S) by 10Ω at a time until the drain voltage is 5V.

24. Record the value of R_S.: _____

Question 6
Why is the decade box's resistance now an optimum value for R_S?

_____

_____

Question 7
Compare your optimum value of R_S with the value used by other groups in the class. What were the lowest and highest values used?

_____

_____

Question 8
What do your findings in the question above tell you about the variations in JFET parameters and the dependency of the self bias circuit on them?

_____

_____

_____

The teacher needs to check your work at this point...

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Student notes

Review questions

Answer these questions to check your understanding of what you have learnt for this chapter. Doing this will also help to prepare you for the tests.

1. What do the letters JFET stand for?

_____

2. What are three advantages of JFETs over BJTs?

_____

3. What are two advantages of BJTs over JFETs?

_____

4. Draw the schematic symbols for an N-channel and P-channel JFET and label each terminal.

5. Why is the JFET called a "voltage-controlled" device?

_____

_____

6. Write the word "positive" or "negative" in the following spaces to make each sentence correct for normal N-channel JFET biasing:

   (a) The gate must be more _____ than the source.

   (b) The drain must be more _____ than the source.

7. State whether the following junctions are forward-biased or reverse-biased when the JFET is operated in an amplifier circuit:

   gate-source junction _____

   gate-drain junction _____

8. Define the following terms:

   (a) $V_{GS(off)}$ _____

   (b) I_{DSS} _____

9. What will happen to the drain-source current of a JFET if the gate-source voltage is changed from -1V to -2V?

   _____

   _____

10. How much gate current flows in a JFET? Why?

    _____

    _____

11. An ohmmeter connected across two terminals of a JFET shows high resistance even when the meter leads are reversed. Is the JFET faulty? Why?

    _____

    _____

12. Explain how the self bias circuit develops a negative gate-source voltage.

    _____

    _____

    _____

Questions 13 to 18 refer to the circuit in Figure 1 below

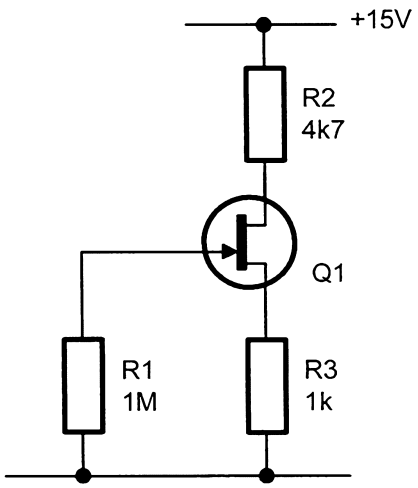

Figure 1

13. What is the gate voltage (V_G)?

14. Calculate the source voltage (V_S) if the gate-source voltage (V_{GS}) is -1.5V.

15. Calculate the drain-source current (I_{DS}).

16. Calculate the drain voltage (V_D).

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17. Calculate the drain-source voltage (V_{DS}).

18. State which component performs the following functions:

    (a) Converts changes in V_{GS} to changes in I_D _____

    (b) Converts changes in I_D to changes in V_D _____

    (c) Holds the gate at zero volts _____

    (d) Develops a source voltage and provides DC feedback _____

Questions 19 to 23 refer to the circuit in Figure 2 below

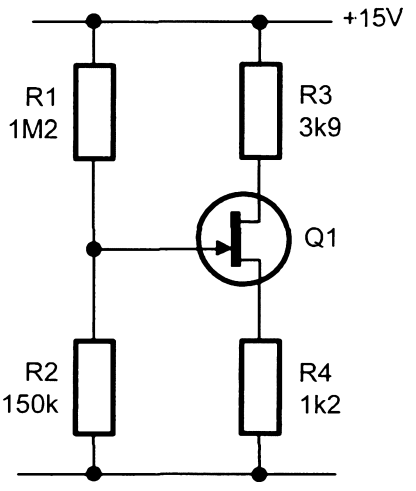

Figure 2

19. Calculate the gate voltage (V_G).

20. Calculate the source voltage (V_S) if the gate-source voltage (V_{GS}) is -0.53V.

21. Calculate the drain-source current (I_{DS}).

22. Calculate the drain voltage (V_D).

23. Calculate the drain-source voltage (V_{DS}).

Questions 24 to 28 refer to the circuit in Figure 3 below

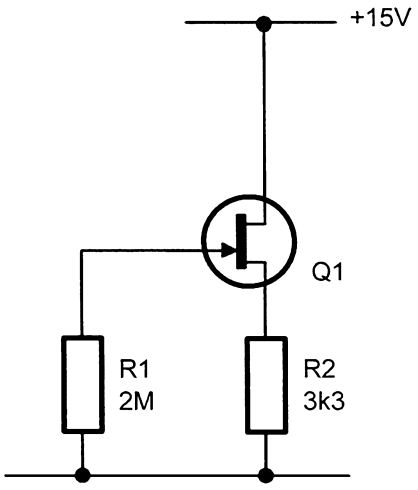

Figure 3

24. What is the gate voltage (V_G)?

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25. Calculate the source voltage (V_S) if the gate-source voltage (V_{GS}) is -6.9V.

26. Calculate the drain-source current (I_{DS}).

27. What is the drain voltage (V_D)?

28. Calculate the drain-source voltage (V_{DS}).

Questions 29 to 35 refer to the circuit in Figure 4 below

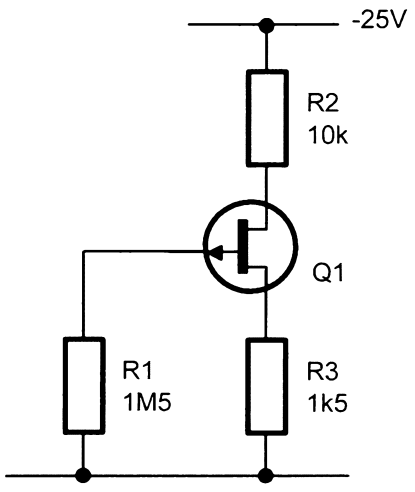

Figure 4

29. What is the gate voltage (V_G)?

30. Calculate the source voltage (V_S) if the gate-source voltage (V_{GS}) is +2.25V.

31. Calculate the drain-source current (I_{DS}).

32. Calculate the drain voltage (V_D).

33. Calculate the drain-source voltage (V_{DS}).

34. Which of the following statements is true?

- ❑ Current flows from common into the JFET's gate.
- ❑ Current flows out of the JFET's gate to common.
- ❑ When gate current flows, drain-source current flows.
- ❑ There is no gate current.

35. Which of the following statements is true?

- ❑ Current flows from common into the JFET's source and out of its drain.
- ❑ Current flows into the JFET's drain and out of its gate to common.
- ❑ The drain current is slightly bigger than the source current.
- ❑ The source current is slightly bigger than the drain current.

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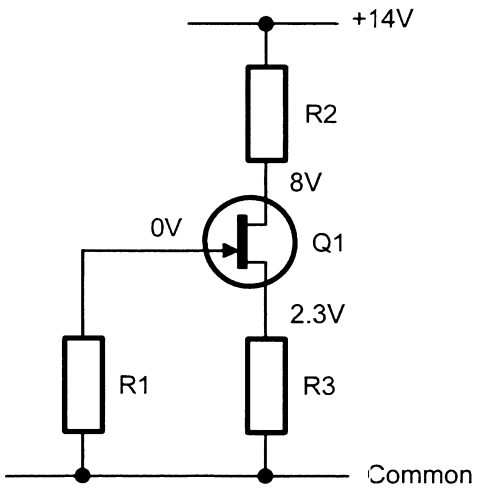

Figure 5

36. Figure 5 above shows a self biased N-channel JFET circuit and its normal quiescent DC voltages. Table 1 below lists the voltages measured around the circuit for six faults. Use this information to determine the likely cause of each fault.

Table 1

V_G	V_S	V_D	Cause
0V	0V	14V	
0V	0V	0V	
3.6V	3.6V	6V	
0V	2.3V	6V	
0V	4V	4V	

Section 7 JFET amplifier configurations and AC parameters

Purpose To develop your knowledge and skills to help you locate amplifier faults by measuring the output signal from a JFET amplifier and comparing it to the predicted output for its configuration and measured input.

Objectives At the end of the lesson you should be able to:

- Identify the three JFET amplifier configurations
- Identify the input and output terminals of each configuration
- Describe the effects on the quiescent voltages and currents around the JFET configurations when an input signal is connected
- State the signal input-output phase relationship for each configuration
- Calculate (using approximation equations) the voltage gain, input resistance and output resistance for the common source amplifier configuration
- Calculate (using approximation equations) the voltage gain, input resistance and output resistance for the common drain amplifier configuration
- State the two factors that determine the maximum peak-to-peak output voltage of a JFET amplifier
- Calculate the maximum peak-to-peak output voltage of a JFET amplifier
- Interpret manufacturers' data on JFETs
- Measure the DC voltages around the circuit of various JFET amplifier circuits
- Measure the gain, phase relationship and maximum peak-to-peak output voltage of a common source and common drain JFET amplifier
- Measure the frequency response of JFET amplifiers

JFET amplifier configurations

Recall that BJT amplifiers can be configured in one of three ways: common emitter, common collector and common base. JFET amplifier circuits can also be configured in one of three ways: common source, common drain and common gate. This chapter examines the AC operation of the common source and common drain configurations.

Common source JFET amplifiers

The circuit of a common source JFET amplifier is shown in Figure 1. The circuit is using self bias and an N-channel JFET.

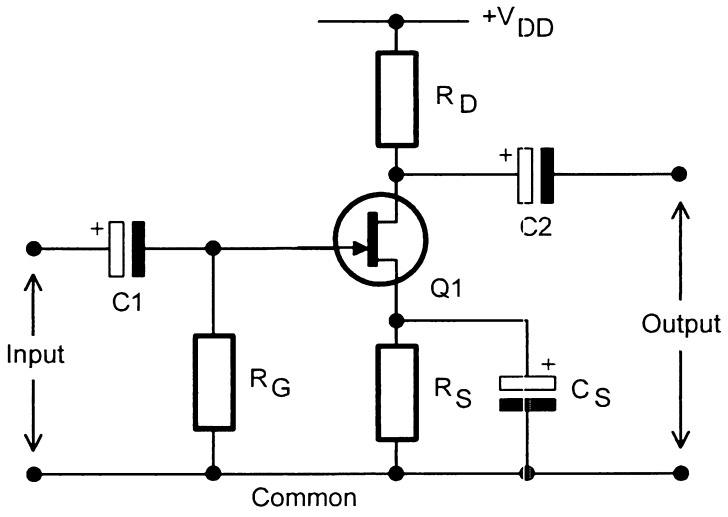

Figure 1 *Common source JFET amplifier*

Before we look at how the circuit works as a voltage amplifier, there's a couple of points that need to be made about it.

First, a source resistor by-pass capacitor (C_S) is included and this will always be the case in the common source JFET circuits analysed in this workbook. To explain, recall that the gain of JFETs is much lower than for BJTs. So, the negative feedback that the source resistor introduces into the circuit will make the circuit's gain even lower (probably less than 2). That being the case, the source resistor by-pass capacitor is essential if the circuit is to have a significant voltage gain.

Second, *C1* and *C2* in Figure 1 are coupling capacitors. They prevent any DC voltages in the source and the load from getting into the amplifier and upsetting its quiescent DC conditions.

How the circuit works as a voltage amplifier

As you know, the DC voltage on the JFET's gate in a self bias circuit is zero volts. And, the voltage on the drain (with respect to common) is some positive voltage less than the supply. Let's say in this example, the drain voltage is 5V.

These quiescent DC conditions are shown in Figure 2 and, without an input signal, they will stay this way for as long as power is connected to the circuit.

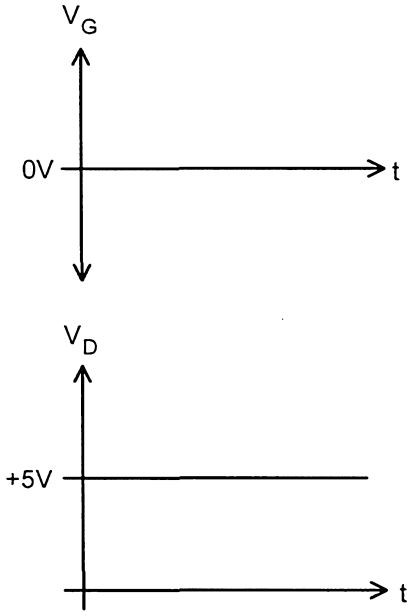

Figure 2

When an AC signal is connected to the amplifier's input, it is superimposed onto the quiescent gate voltage (see Figure 3). This causes the JFET's gate voltage to go up and down.

As the input signal increases towards its positive peak, the gate voltage (V_G) gets closer in value to the source voltage (V_S). In other words, the gate-source voltage (V_{GS}) goes down (or becomes less negative). This decrease in gate-source voltage causes an increase in drain-source current which increases the potential difference across the drain resistor and decreases the voltage on the drain with respect to common.

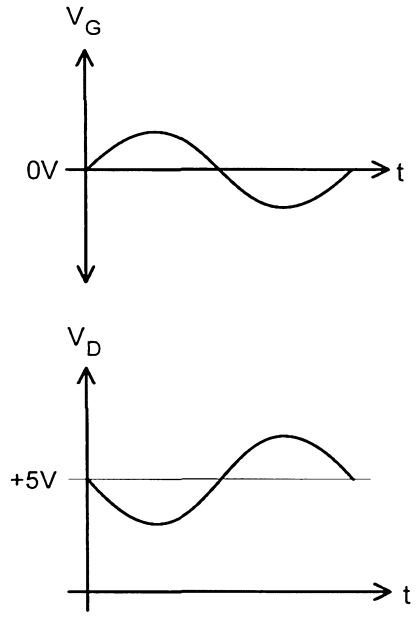

Figure 3

Then, as the input signal reverses direction and heads towards its negative peak, the gate voltage (V_G) gets further away in value from the source voltage (V_S). In other words, the gate-source voltage (V_{GS}) goes up (or becomes more negative). This increase in gate-source voltage in the negative direction causes a decrease in drain-source current which decreases the potential difference across the drain resistor and increases the voltage on the drain with respect to common.

The result is a varying DC voltage on the drain that is a phase-inverted copy of the input signal and up to 100 times larger.

Output resistance

Again, if you consider the circuit in Figure 6, the resistance between the two output terminals appears to be the simple parallel combination of R_D and the resistance of the current source. However, the ideal resistance of a current source is infinity and in practice usually very large. That being the case, the equation for the output resistance is:

$$Rout = R_D$$

Voltage gain

The equation for calculating the common source configuration's theoretical voltage gain is derived by applying a little algebra to the general equation for voltage gain: $Av_{(unloaded)} = \frac{Vout}{Vin}$.

If you consider the diagram in Figure 6, you can see that from an AC perspective the amplitude of the output signal must be the same as the amplitude of the AC voltage across the drain resistor. Using Ohm's Law, the AC voltage across the drain resistor is: $i_{DS} \times R_D$.

Substituting $i_{DS} \times R_D$ for *Vout* in the general gain equation gives: $Av_{(unloaded)} = \frac{i_{DS} \times R_D}{Vin}$.

Similarly, it can be seen that the amplitude of the input signal must be the same as the amplitude of the AC voltage between the JFET's gate and source (v_{GS}).

Substituting v_{GS} for *Vin* in the modified gain equation above gives: $Av_{(unloaded)} = \frac{i_{DS} \times R_D}{v_{GS}}$.

Now, to simplify this equation further, you need to know a little bit more about the JFET's transconductance. It is an electrical property of the JFET that is specified by the manufacturer in the same way that beta is for BJTs.

Transconductance describes the relationship between changes in the gate-source voltage (V_{GS}) and the resulting changes in the drain-source current (I_{DS}). Mathematically, it's expressed as:

$$Gm = \frac{\Delta I_{DS}}{\Delta V_{GS}}$$

Notice that the transconductance describes a relationship between current and voltage that is the opposite of resistance (ie $R = \frac{V}{I}$). The opposite of resistance is conductance, the standard unit for which is the Siemen (*S*). A typical figure for the transconductance of a JFET is 5,000µS. Importantly, the larger the JFET's transconductance, the greater its gain.

If the mathematical expression for transconductance is transposed and *delta* (Δ) is left off, the equation becomes: $i_{DS} = Gm \times v_{GS}$.

If this expression is substituted for i_{DS} in the modified gain equation, it becomes: $Av_{(unloaded)} = \frac{Gm \times v_{GS} \times R_D}{v_{GS}}$.

Finally, simplifying this expression by cancelling out v_{GS} gives:

$$Av_{(unloaded)} = Gm \times R_D$$

Note: Test questions will not ask you to show how this equation is derived.

The effects of loading on the common source configuration

To understand the effects of a load on the common source configuration consider how the AC equivalent circuit changes with a load connected (see Figure 7 below).

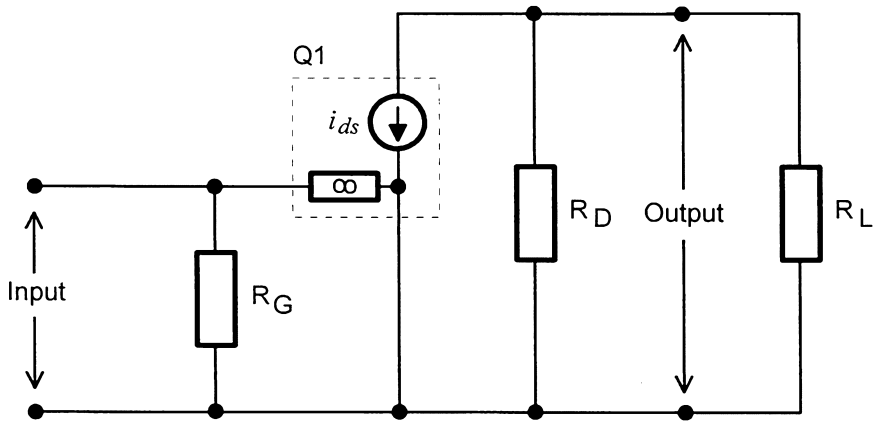

Figure 7 *The AC equivalent circuit of the common source configuration with a load resistor connected*

It is clear from the diagram that the drain resistor and the load resistor are connected in parallel with each other. This means that the gain equation changes from $Av = Gm \times R_D$ to:

$$Av_{(loaded)} = Gm \times (R_D // R_L)$$

An important point to note here is that the load only affects the amplifier's voltage gain. It **doesn't** change its input resistance or output resistance.

Practise calculating the AC parameters of the common source configuration by trying the following questions.

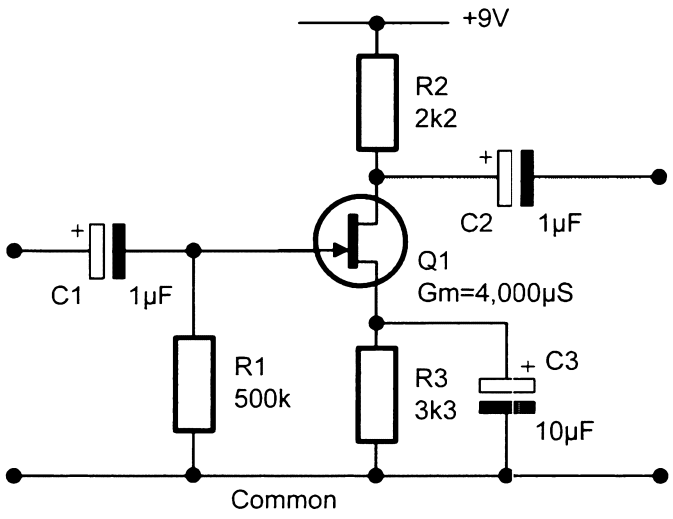

Figure 8

1. Calculate the unloaded voltage gain of the amplifier in Figure 8.

2. What is the input resistance?

3. What is the output resistance?

4. Calculate the loaded voltage gain of the amplifier with a 3kΩ load.

5. What will happen to the voltage gain (either unloaded or loaded) if the JFET is replaced with one having a transconductance of 7,500μS?

Common drain JFET amplifiers

The circuit of a common drain JFET amplifier is shown in Figure 9. The circuit is using self bias and an N-channel JFET. A source resistor by-pass capacitor cannot be used with this circuit because it would short-circuit the AC output signal to common.

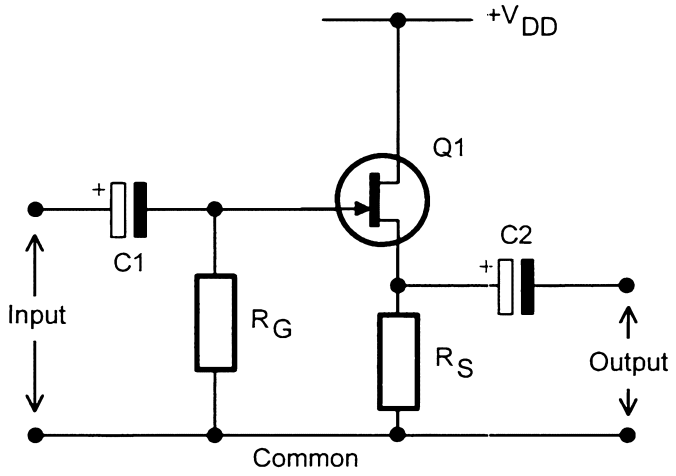

Figure 9 *Common drain JFET amplifier*

How the circuit works as a voltage amplifier

As you know, the DC voltage on the JFET's gate in a self bias circuit is zero volts. And, the voltage on the source (with respect to common) is some positive voltage less than the supply. Let's say in this example, the source voltage is 5V.

These quiescent DC conditions are shown in Figure 10 and, without an input signal, they will stay this way for as long as power is connected to the circuit.

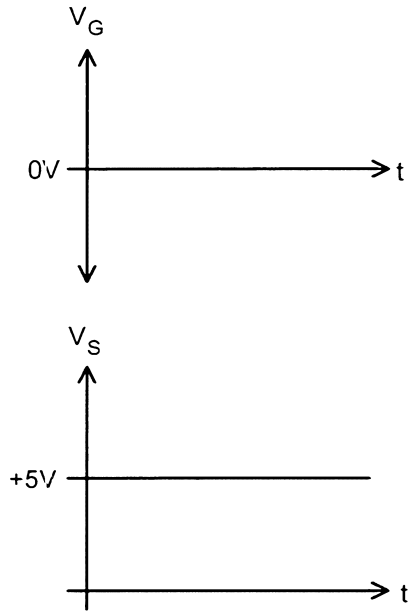

Figure 10

When an AC signal is connected to the amplifier's input, it is superimposed onto the quiescent gate voltage (see Figure 11). This causes the JFET's gate voltage to go up and down.

As the input signal increases towards its positive peak, the gate voltage (V_G) gets closer in value to the source voltage (V_S). In other words, the gate-source voltage (V_{GS}) goes down (or becomes less negative). This decrease in gate-source voltage causes an increase in drain-source current which increases the potential difference across the source resistor as shown in Figure 11.

Then, as the input signal reverses direction and heads toward its negative peak, the gate voltage (V_G) gets further away in value from the source voltage (V_S). In other words, the gate-source voltage (V_{GS}) goes up (or becomes more negative).

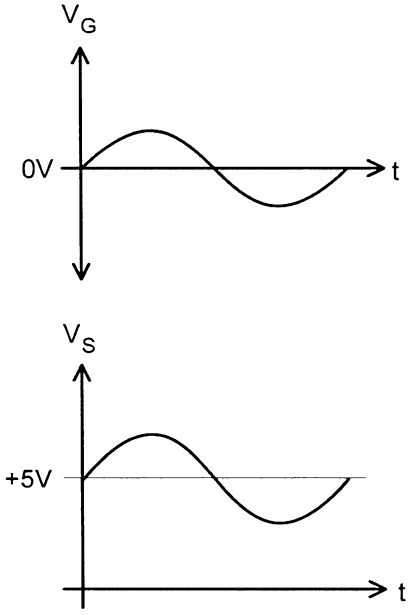

Figure 11

This increase in gate-source voltage causes a decrease in drain-source current which decreases the potential difference across the source resistor.

The result is a varying DC voltage on the source that is an in-phase copy of the input signal and a little smaller than it.

Common drain amplifier parameters

From an AC perspective, the common drain amplifier in Figure 9 looks like the diagram in Figure 12 below.

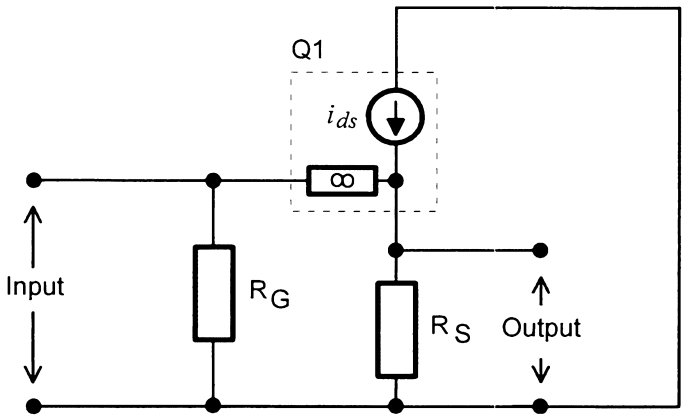

Figure 12 *The AC equivalent circuit of the common drain amplifier in Figure 9*

This circuit can be used to help show how the equations for the AC parameters are derived. (**Note:** Test questions will not ask you to draw this circuit.)

Input resistance

If you consider the diagram in Figure 12, the resistance between the two input terminals can be seen to be the gate resistor connected in parallel with an infinitely large resistance that is in series with the source resistor. That being the case, the equation for the input resistance is:

$$Rin = R_G$$

Output resistance

Again, if you consider the diagram in Figure 12, the resistance between the two output terminals appears to be only the source resistor. However, determining the output resistance is a little more complicated. Luckily, there is a simple and convenient method of approximating the output resistance for small signal common drain JFET amplifiers and the equation is shown below.

$$Rout \approx \frac{1}{Gm}$$

Note: The smaller the value of R_S the less accurate this approximation becomes.

Voltage gain

The equation for calculating the common drain configuration's voltage gain is derived by applying a little algebra to the general equation for voltage gain: $Av_{(unloaded)} = \frac{Vout}{Vin}$.

If you consider the diagram in Figure 12, you can see that from an AC perspective the amplitude of the output signal must be the same as the amplitude of the AC voltage across the source resistor. Using Ohm's Law, the AC voltage across the source resistor is: $i_{DS} \times R_S$.

Substituting $i_{DS} \times R_S$ for $Vout$ in the general voltage gain equation gives: $Av_{(unloaded)} = \frac{i_{DS} \times R_S}{Vin}$.

Similarly, it can be seen that the amplitude of the input signal must be the same as the sum of the AC voltages across the gate-source connection of the JFET (v_{GS}) and the source resistor (v_{RS}); in other words, $v_{GS} + v_{RS}$.

Substituting $v_{GS} + v_{RS}$ for Vin in the modified gain equation above gives: $Av_{(unloaded)} = \frac{i_{DS} \times R_S}{v_{GS} + v_{RS}}$.

Furthermore, substituting $i_{DS} \times R_S$ for v_{RS} in the equation gives: $Av_{(unloaded)} = \frac{i_{DS} \times R_S}{v_{GS} + (i_{DS} \times R_S)}$.

And, substituting $Gm \times v_{GS}$ for i_{DS} in the equation gives: $Av_{(unloaded)} = \frac{Gm \times v_{GS} \times R_S}{v_{GS} + (Gm \times v_{GS} \times R_S)}$.

Finally, simplifying this expression by cancelling out v_{GS} gives:

$$Av_{(unloaded)} = \frac{Gm \times R_S}{1 + (Gm \times R_S)}$$

Note: Test questions will not ask you to show how this equation is derived.

Practise calculating the AC parameters of the common drain configuration by trying the following questions.

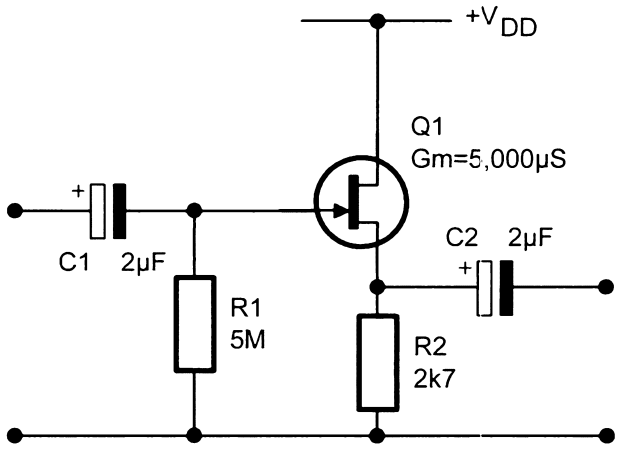

Figure 13

1. Calculate the unloaded gain of the common drain JFET amplifier in Figure 13.

2. What is the input resistance?

3. Calculate the approximate output resistance.

The effects of loading on the common drain configuration

As the output resistance of the common drain configuration is so low, it is safe to say that for most purposes, the effect of connecting a load is so small that it can be ignored. That being the case, we can say that the loaded voltage gain is the same as the unloaded voltage gain.

Calculating the maximum peak-to-peak output and input voltages

Like BJT amplifiers, there are two factors that affect the maximum peak-to-peak output voltage of an unloaded FET amplifier. These are:

- the size of the supply voltage; and
- the quiescent DC voltage on the JFET's terminal that the output is taken from.

These are shown on the circuits of a common source and common drain JFET amplifiers in Figure 14 below.

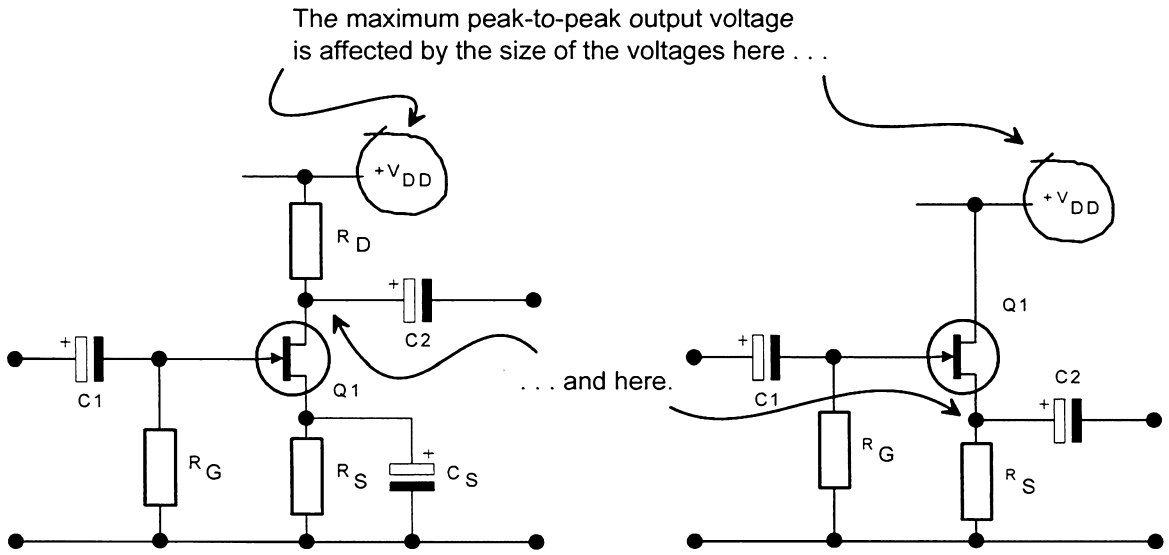

Figure 14 *The maximum peak-to-peak output voltage before clipping is affected by the supply voltage and the quiescent DC voltage on the drain (of the common source JFET amplifier) or the source (of the common drain JFET amplifier)*

To calculate the maximum peak-to-peak output voltage for unloaded JFET amplifiers you must first compare the quiescent DC voltage on the output lead of the FET to the supply voltage. If the voltage on the output lead is less than half of the supply voltage then the maximum peak-to-peak output voltage is found using the equation:

Common source: $Vout_{(max)} = V_D \times 2$

Common drain: $Vout_{(max)} = V_S \times 2$

If the voltage on the output lead is more than half of the supply voltage then the maximum peak-to-peak output voltage is found using the equation:

Common source: $Vout_{(max)} = (V_{DD} - V_D) \times 2$

Common drain: $Vout_{(max)} = (V_{DD} - V_S) \times 2$

Once the maximum peak-to-peak output voltage before clipping is known, the maximum input voltage can be found using the equation:

$$Vin_{(max)} = \frac{Vout_{(max)}}{Av}$$

Note: This discussion on maximum peak-to-peak output voltage and these equations assume an amplifier that is not loaded or only relatively lightly loaded. The analysis becomes more complicated for more heavily loaded amplifiers but this won't be dealt with here.

Manufacturers' data

Table 1 shows relevant data on some commonly available JFETs.

Table 1

Type	Case	$-V_{GS}$ (off)		I_{DSS} (mA)		Gm (µS)		Power (mW)	Use/Comments
		Min	Max	Min	Max	Min	Max		
BF245	TO-92*	0.5	8	6	15	3,000	6,500	300	N/Ch Junction Audio to HF
BF998	SMT		2.5	2	18	24,000 typ		200	VHF/UHF Dual Gate SMT
BFR84	TO-72*	1.5	3.8	20	55	15,000 typ		300	VHF Dual Gate
MPF102	TO-92*	0.5	8	2	20	2,000	7,500	310	N/Ch Junction - VHF
MPF105	TO-92*		8	4	16	2,000	6,000	310	N/Ch Junction - Audio
MPF106	TO-92*	0.5	4	4	10	2,500	7,000	310	N/Ch Junction - RF
2N4342	TO-92*		5	12	30		6,000	180	P/Ch Junction - Audio
2N5245	TO-92*	1.5	6	1	18	5,800 typ		360	N/Ch VHF/UHF Mixer
2N5459	TO-92*	2	8	4	9	2,000	6,000	310	N/Ch Junction Audio
2N5484	TO-92*	0.3	3	1	5	3,000	6,000	310	N/Ch Junction VHF
2N5485	TO-92*	0.5	4	4	10	3,500	7,000	310	N/Ch Junction VHF
2N5486	TO-92*	2	6	8	20	4,000	8,000	310	N/Ch Junction VHF

* There is more than one variation of this package

Substituting JFETs

Most of the notes in Section 5 that are related to substituting BJTs are applicable to JFETs. When choosing a suitable substitute by comparing JFET data, the key electrical properties that should be matched include:

- the maximum allowable drain-source voltage ($V_{DS(max)}$);
- the maximum allowable drain current ($I_{D(max)}$);
- the maximum power dissipation ($P_{(max)}$);
- the gate-source voltage that turns the device off ($V_{GS(off)}$); and to a lesser extent
- the *transconductance* (*Gm*).

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Student notes

Skill practice 7

Practise measuring AC voltages in FET amplifiers using an oscilloscope to determine input-output phase relationship, voltage gain and frequency response

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 1½ hours to complete this exercise.

Equipment

- Emona Trainer
- DMM
- decade resistance box
- 2N5485 JFET
- 1MΩ ¼W resistor
- 2k2Ω ¼W resistor
- 10µF capacitor
- two 1µF capacitor
- three BNC to alligator-clip leads
- banana leads
- hook-up wire
- wire strippers

Remember:

Follow TAFE NSW WHS guidance at all times!

Work tasks

1. Read your WHS responsibilities at the top of the form below. Then conduct a WHS risk assessment and record your findings in the space provided.

Responsibilities of students under the Model WHS Act: s28

- Take reasonable care for your own health and safety by working safely at all times
- Take reasonable care to ensure that your acts or omissions don't put the health and safety of others at risk
- Follow all TAFE NSW WHS guidance and comply with all reasonable instructions from TAFE NSW staff to assist them in complying with the TAFE NSW WHS requirements
- In addition to the above, you must:
  - use and maintain machinery, tools and all other equipment properly and safely
  - ensure that your work area is free of hazards
  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

Risks involved in this activity include:	**Control measures:**
Trip hazards (eg students bags) Objects dropped on feet (while equipment is taken to and from workbenches).	Move bags and other objects from walkways Plan lifting of equipment
Others: _____	Other: _____
_____	_____
_____	_____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

3. Turn off the Emona Trainer then wire the circuit of Figure 1.

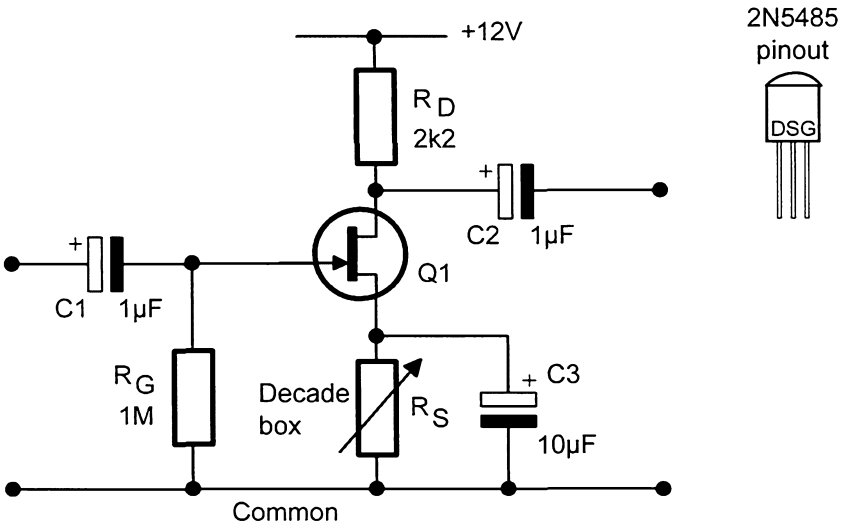

Figure 1

4. Set the decade resistance box to 600Ω.

5. Turn on the Emona Trainer.

6. Change the decade box's value by 10Ω at a time, until the voltage on the drain (V_D) is 7V. Use the DMM to measure the drain voltage.

7. Set the signal generator for a 1kHz sinewave and connect it to the input of the amplifier.

8. Connect channel 1 of the CRO to the input of the amplifier and channel 2 to the output.

9. Adjust the CRO so that both channels are displayed. If the output is clipped, reduce the amplitude of the input signal.

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10. Measure the input and output voltages. Record your measurements in Table 1.

11. Use these measured voltages to calculate and record the amplifier's voltage gain.

12. Observe and record the input-output signal phase relationship.

Table 1

Input voltage	Output voltage	Voltage gain	Input-output phase relationship

Question 1
Calculate the amplifier's theoretical voltage gain assuming the JFET has a *Gm* of 3,500μS.

Question 2
Compare your theoretical gain that you just calculated with the measured gain. Are they close in value? What might explain differences between the two?

Question 3
Why is the amplifier's voltage gain so low (compared to the common emitter BJT amplifier) even with a source resistor by-pass capacitor connected?

The teacher needs to check your work at this point...

13. Determine the amplifier's theoretical maximum peak-to-peak output voltage. Record the value in Table 2 below.

14. Find the amplifier's maximum peak-to-peak output voltage by increasing the amplitude of the input signal until the output signal is just about to clip (at the top). Record your measurement in Table 2.

Table 2	Theoretical	Measured
Maximum peak-to-peak output voltage		

Question 4
What is the maximum peak-to-peak input voltage allowable before the signal source starts to overdrive the amplifier?

Question 5
Which two circuit voltages determine the amplifier's maximum peak-to-peak output voltage?

15. Momentarily remove *C3* and note the effect on output voltage and voltage gain.

Question 6
Why does the output voltage go down when you remove *C3*?

The teacher needs to check your work at this point...

16. Reconnect *C3*.

17. Measure the amplifier's *f1* and *f2*. Record your measurements in Table 3 below.

    Tip: Remember that to find *f1* you reduce the frequency of the amplifier's input signal and to find *f2* you increase its frequency until the amplitude of the output voltage drops to 0.707 of its mid-band output voltage.

    Another tip: Before you adjust the frequency of the input signal, make things easier for yourself by first adjusting its amplitude so that the amplifier's output is seven divisions peak-to-peak (and not clipped).

Table 3

f1	*f2*

The teacher needs to check your work at this point...

There's more steps on the next page...

18. Disconnect the DC power supply and the signal generator.

19. Modify your JFET amplifier to a common drain type as shown in Figure 2.

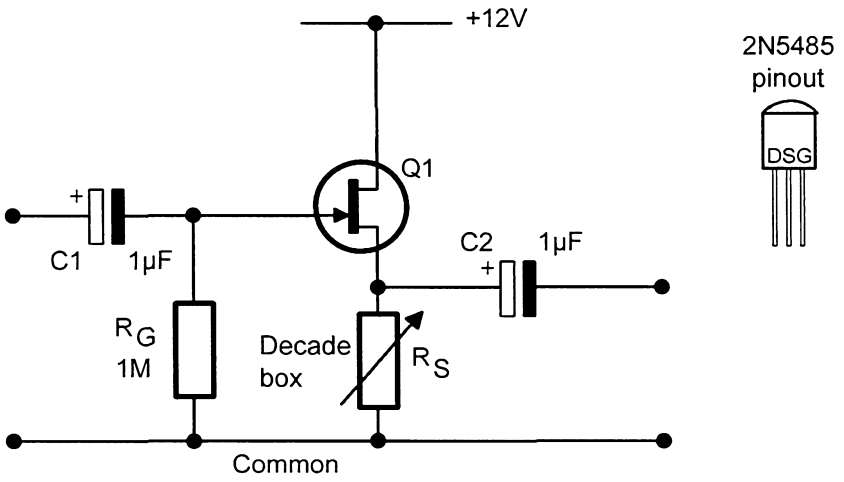

Figure 2

20. Adjust the decade box so that the source resistance is 10kΩ.

21. Set the signal generator for a 1kHz sinewave and connect it to the amplifier's input.

22. Connect channel 1 of the CRO to the input of the amplifier and channel 2 to the output.

23. Adjust the CRO so that both channels are displayed. If the output is clipped, reduce the amplitude of the input signal.

24. Measure the input and output voltages. Record your measurements in Table 4.

25. Use these measured voltages to calculate and record the amplifier's voltage gain.

26. Observe and record the input-output signal phase relationship.

Table 4

Input voltage	Output voltage	Voltage gain	Input-output phase relationship

Question 7
Calculate the amplifier's theoretical voltage gain assuming the JFET has a *Gm* of 3,500μS.

Question 8
Compare your theoretical gain that you just calculated with the measured gain. Are they close in value? What might explain differences between the two?

Question 9
Why doesn't this configuration have a source resistor by-pass capacitor connected?

The teacher needs to check your work at this point...

27. Disconnect the input signal and measure the source voltage (V_S) with a DMM.

28. Use this measurement to determine the amplifier's theoretical maximum peak-to-peak output voltage. Record the value in Table 5 on the next page.

29. Reconnect the input signal.

30. Find the amplifier's maximum peak-to-peak output voltage by increasing the amplitude of the input signal until the output signal is just about to clip. Record your measurement in Table 5.

Table 5	Theoretical	Measured
Maximum peak-to-peak output voltage		

Question 10
What is the maximum peak-to-peak input voltage allowable before the signal source starts to overdrive the amplifier?

_____

_____

Question 11
Which two circuit voltages determine the amplifier's maximum peak-to-peak output voltage?

_____

_____

31. Measure the amplifier's *f1* and *f2*. Record your measurements in Table 6 below.

Tip: Before you adjust the frequency of the input signal, make things easier for yourself by first adjusting its amplitude so that the amplifier's output is seven divisions peak-to-peak (and not clipped).

Table 6

f1	*f2*

The teacher needs to check your work at this point...

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Student notes

Review questions

Answer these questions to check your understanding of what you have learnt for this chapter. Doing this will also help to prepare you for the tests.

Questions 1 to 10 refer to the circuit in Figure 1 below

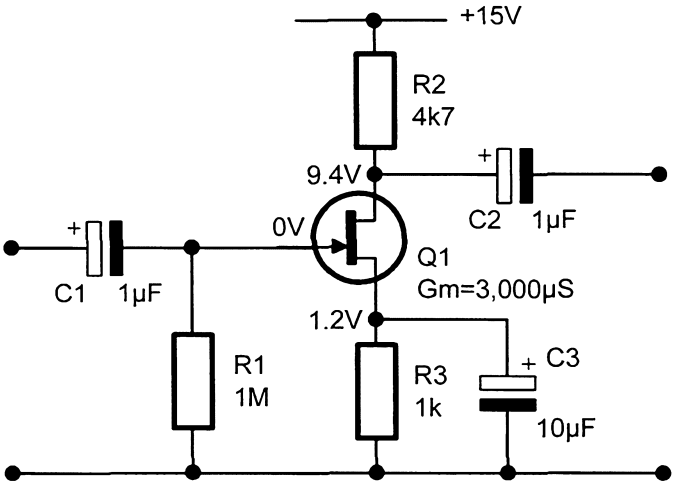

Figure 1

1. What configuration is the amplifier?

2. What is the amplifier's input-output signal phase relationship?

3. Calculate the unloaded voltage gain.

4. What is the input resistance?

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5. What is the output resistance?

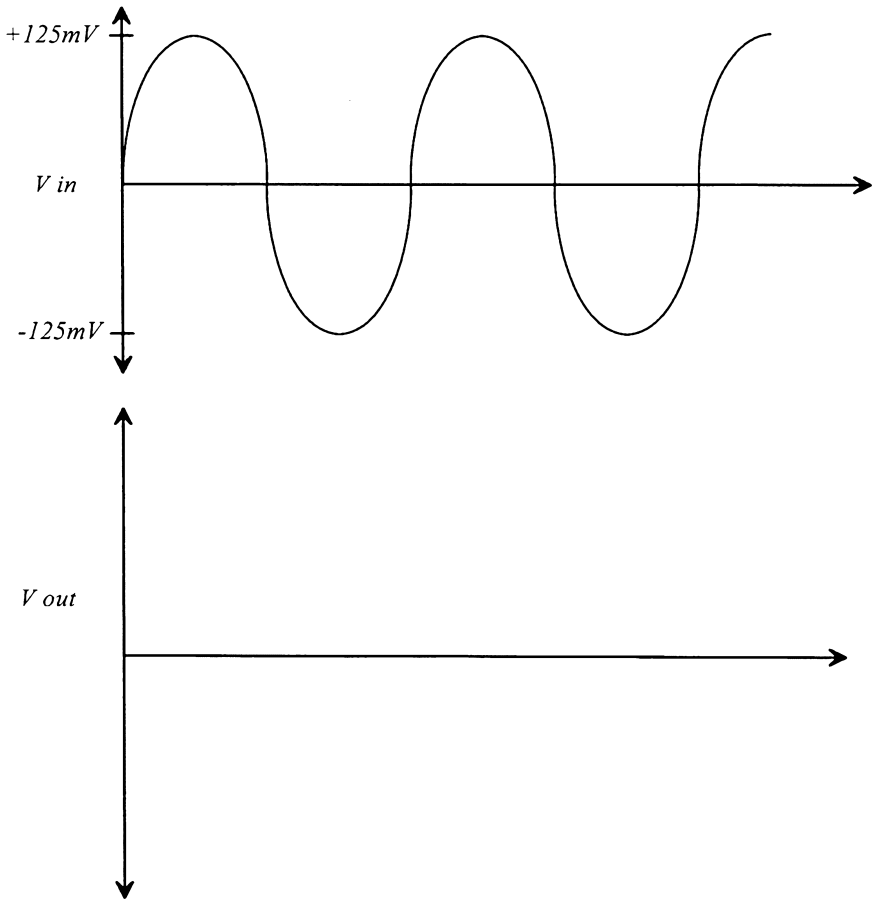
6. Determine the maximum peak-to-peak output voltage before clipping.

7. Calculate the amplifier's maximum peak-to-peak input signal before clipping of the output.

8. What would happen to the amplifier's voltage gain if the capacitor *C3* became an open-circuit?

9. What is the purpose of *C1* and *C2*?

10. Draw what you would expect to see at the amplifier's output for the input signal shown on the graph below.



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Questions 11 to 15 refer to the circuit in Figure 2 below

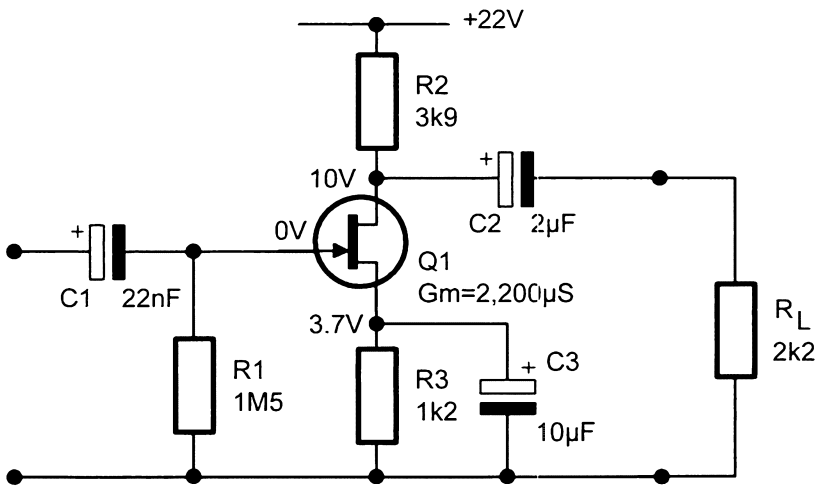

Figure 2

11. Calculate the unloaded voltage gain.

12. Calculate the loaded voltage gain.

13. What is the input resistance?

14. What is the output resistance?

15. What will happen to the loaded output voltage if the load resistance increased?

Questions 16 to 25 refer to the circuit in Figure 3

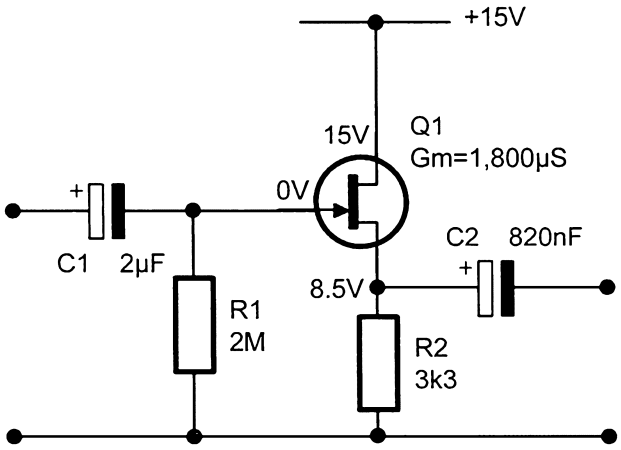

Figure 3

16. What configuration is the amplifier?

17. What is the amplifier's input-output signal phase relationship?

18. Calculate the unloaded voltage gain.

19. What is the input resistance?

20. Calculate the approximate output resistance.

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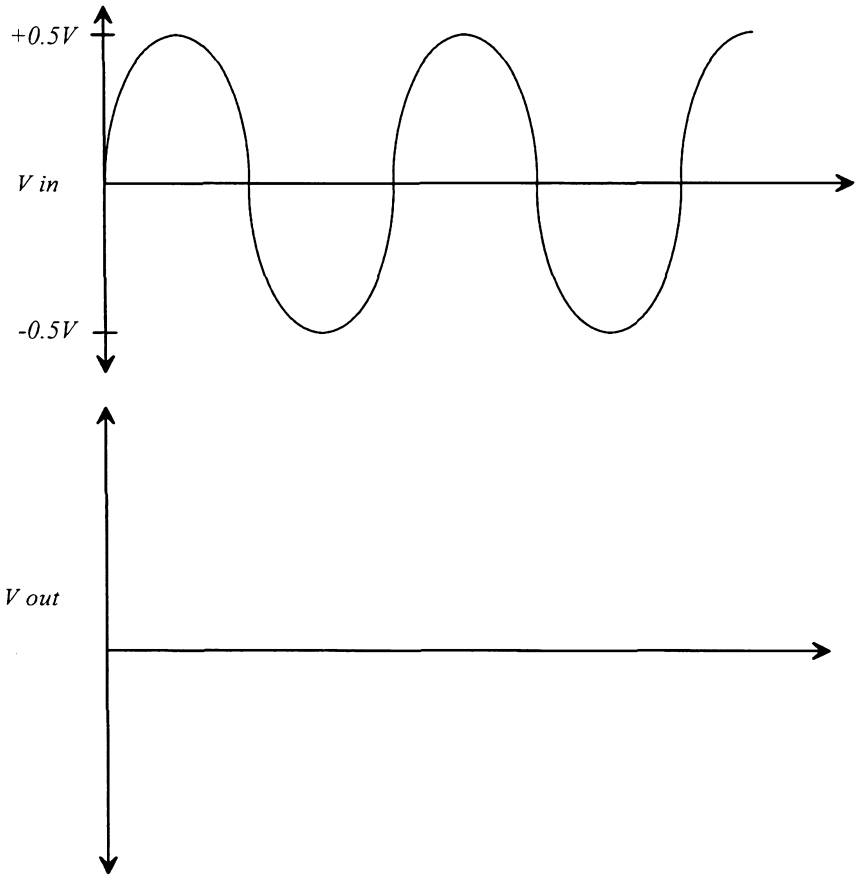
21. Determine the maximum peak-to-peak output voltage before clipping.

22. Calculate the maximum peak-to-peak input signal before clipping of the output.

23. What would happen to the amplifier's voltage gain if a load resistor was connected?

24. What is a practical use of this amplifier stage considering it has a voltage gain of less than 1?

25. Draw what you would expect to see at the amplifier's output for the input signal shown on the graph on the next page.



more questions on the next page . . .

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Questions 26 to 28 refer to the circuit in Figure 4

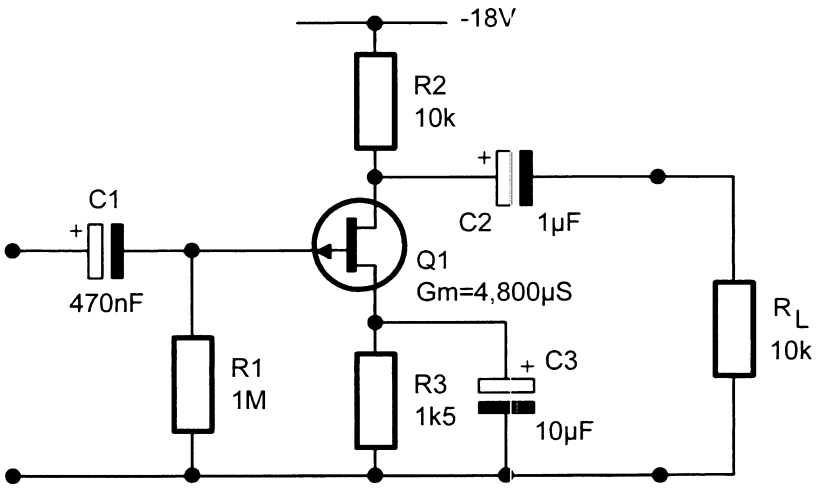

Figure 4

26. Calculate the loaded voltage gain.

27. What is the input resistance?

28. Calculate the approximate output resistance.

Section 8 MOSFET amplifiers

Purpose To develop your understanding of the principles of operation, biasing methods and configurations of MOSFETs so that you can predict and measure DC and AC voltages around MOSFET amplifiers.

Objectives At the end of the lesson you should be able to:

- Draw and identify the schematic symbols for depletion and enhancement mode MOSFETs
- Describe the bias conditions needed for each junction of a MOSFET for it to operate in amplifier circuits
- Show the direction of current flow and voltage polarity at each terminal of the MOSFET
- Explain the operating principles of MOSFETs
- Interpret graphs for MOSFET input-output transfer characteristics
- Identify the similarities and differences between MOSFET and JFET biasing circuits
- Calculate the voltages around MOSFET biasing circuits
- Identify the similarities and differences between MOSFET and JFET amplifier configurations
- Calculate the voltage gain, input resistance and output resistance of common source and common drain MOSFET amplifiers
- Measure the DC voltages around the circuit of various MOSFET amplifier circuits
- Measure the gain, phase relationship and maximum peak-to-peak output voltage of a common source and common drain MOSFET amplifier
- Measure the frequency response of MOSFET amplifiers

Introduction

JFETs are one of two superordinate classes of field effect transistor; the other is the MOSFET (Metal Oxide Semiconductor FET). There are many discrete component variations of MOSFETs nowadays including; VMOS (V-channel MOSFET), TMOS (T-channel MOSFET), Dual Gate FETs, IGBTs (Insulated Gate Bipolar Transistors) and HEXFETs. MOSFETs are much more widely used than JFETs, especially in power applications. In this chapter we'll introduce you to the basic MOSFET design which you can use as a springboard to learning about other MOSFET technologies as required.

Metal Oxide Semiconductor FETs

The MOSFET is like a JFET with an insulated gate. There are two basic kinds of MOSFET:

- depletion mode; and
- enhancement mode.

Both are available in N-channel/type and P-channel/type. Circuits that make use of both types of MOSFET (such as some logic families) are said to be "complementary" which gives us the "C" in CMOS (as in CMOS logic gates.)

Depletion mode MOSFETs

The depletion mode MOSFET is available in either N-channel or P-channel and can be compared with N-channel and P-channel JFETs. Their schematic symbols and representative physical construction are shown in Figures 1 and 2. Like JFETs, the three terminals are called drain, gate and source.

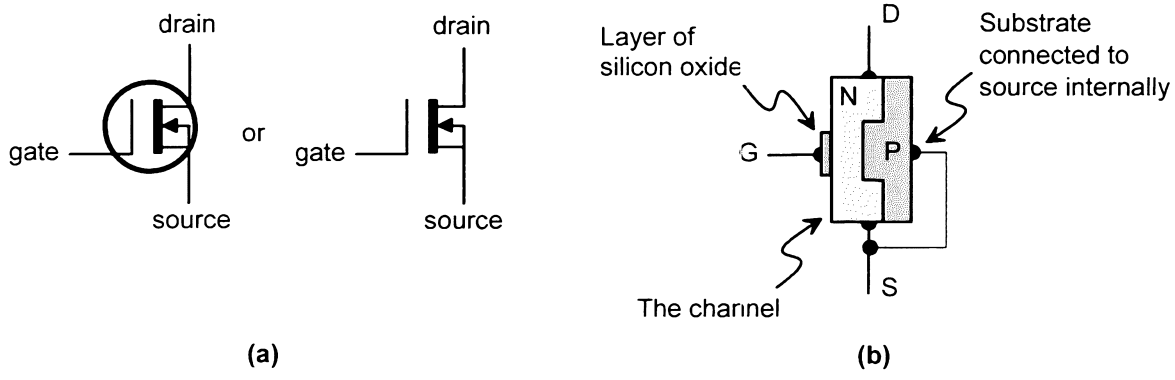

Figure 1 *(a) Schematic symbol of an N-channel depletion mode MOSFET; and (b) cross-sectional view of its construction*

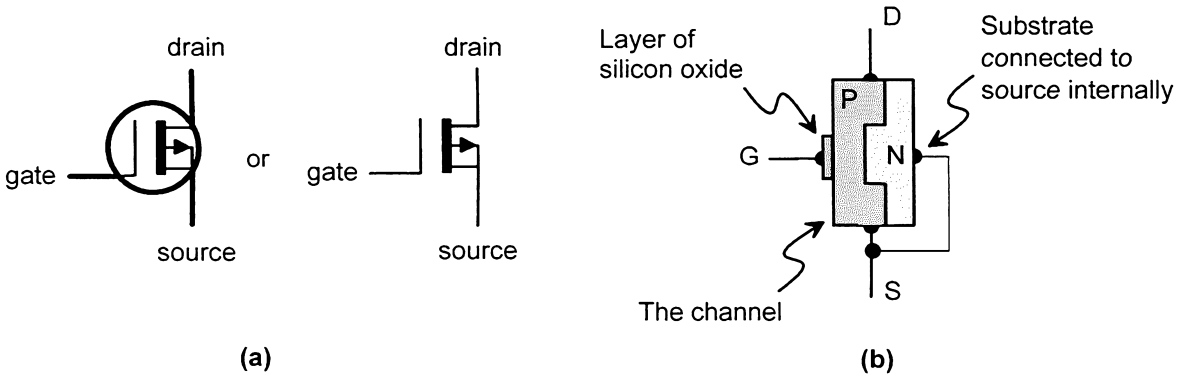

Figure 2 *(a) Schematic symbol of a P-channel depletion mode MOSFET; and (b) cross-sectional view of its construction*

The constructional diagram for each MOSFET (Figures 1b and 2b) shows how the devices get their name. The N-channel MOSFET has a piece of n-type doped silicon material connecting the drain and source which acts as a channel in a similar way to the JFET. The P-channel MOSFET has exactly the same construction with the channel being made from p-type material and the substrate n-type material.

Although MOSFETs are similar to JFETs in that they have a channel, you have probably noticed two differences. First, the MOSFET's channel sits on a *substrate* (or foundation) of material doped in the opposite polarity to the channel. Second, where the JFET's gate connects directly to the channel, the MOSFET's gate is connected to the channel by a very thin layer of silicon oxide (SiO_2).

Connecting the gate to the channel in this way insulates the gate from the rest of the MOSFET so only extremely small amounts of current can flow into the gate (in other words, leakage current). That being the case, the input resistance is extremely big. In fact, it can exceed 1,000MΩ! The insulating effect of the layer of silicon oxide is the reason why MOSFETs are sometimes called *Insulated Gate* FETs or IGFETs.

Handling Precautions

Unfortunately, having this very thin layer of silicon oxide between the gate and the channel also has a disadvantage. MOSFETs are easily damaged by static electricity. In fact, they are so susceptible to electro-static discharge (ESD) that they can be degraded or destroyed by static discharges that you're not even aware of! There doesn't have to be an electro-static "belt" or spark for the damage to be done.

That being the case, whenever you're handling MOS devices (including ICs) you need to follow some basic precautions.

- MOSFETs should be stored and shipped using ESD control measures.
- All instruments and metal benches should be properly earthed when connecting or testing MOSFETs.
- An earthing strap to electrical ground should be connected to the technicians body and all work should be done on a conductive mat.
- Never remove the MOSFET device from the circuit while the power is on.
- Do not apply signals while the DC power is off.

Depletion mode MOSFET operation

It is useful to describe the operation of the depletion mode MOSFET by comparing it to the JFET's operation because they're the same in several ways. Like the JFET, the drain-source connection can be notionally thought of as a resistor. So, if a potential is applied between the drain and source, a drain-source current (I_{DS}) flows even with a gate-source voltage of zero. This is shown using an N-channel MOSFET Figure 3 below.

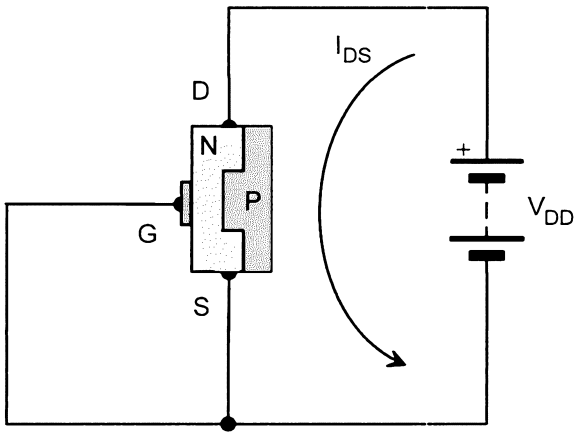

Figure 3 *Drain-source current flows even with a gate-source voltage of zero*

The amount of drain-source current that would flow would be affected by the channel's effective resistance.

Recall that the biasing conditions for a JFET set-up the gate so that it is negative with respect to the source. The depletion mode MOSFET can be biased in the same way (see Figure 4 below).

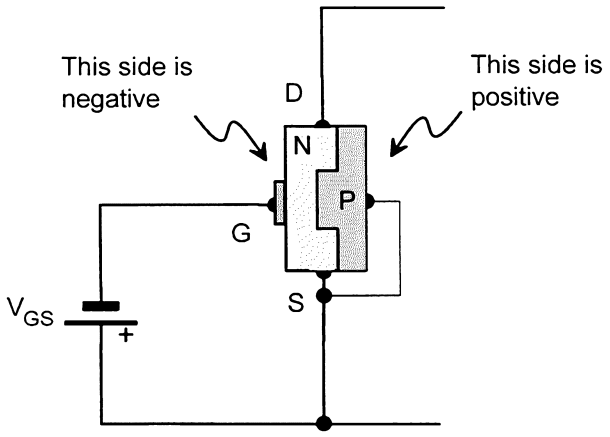

Figure 4 *When the gate is made negative with respect to the source a charge is developed across the channel and the substrate because the substrate is connected to the source internally*

Recall also that variations in the gate-source voltage of the JFET cause variations in drain-source current and, while this also describes the operation of the depletion mode MOSFET, it happens for a different reason. To explain, remember that a depletion layer always forms across a p-n junction. This is shown for an N-channel MOSFET in Figure 5 with a gate-source voltage of zero.

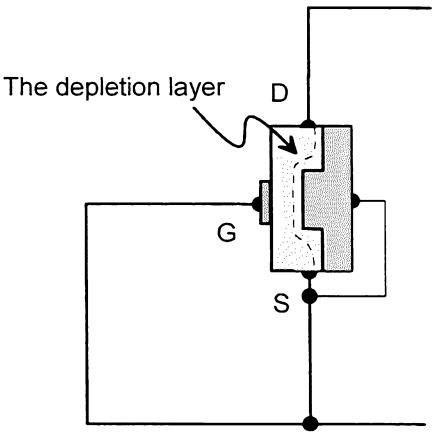

Figure 5 *A depletion layer develops at the junction of the channel and the substrate*

When the gate is made negative with respect to the source as shown in Figure 6 (or positive for the P-channel depletion mode MOSFET) the negative charge on the gate repels free electrons in the channel away from the gate area toward the p-n junction.

At the same time, the relative positive charge on the substrate attracts free electrons in the p-type material toward it. This causes the holes in the p-type material to move toward the p-n junction also. The extra free electrons near the p-n junction match up with the extra holes in this region and so the depletion layer gets bigger as shown in Figure 6 below.

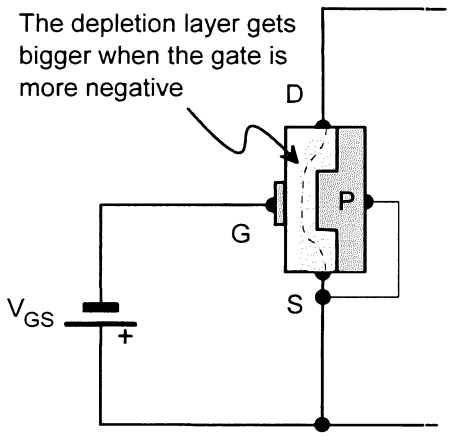

Figure 6 *When the gate is made negative with respect to the source, the depletion layer effectively gets bigger*

This means that the channel effectively becomes thinner and hence more resistive. This in turn reduces the drain-source current.

Like JFETs, if the gate is made sufficiently negative with respect to the source, the MOSFET's depletion layer becomes so big that no drain-source current can flow.

Note: It might be tempting to think that, as the substrate is p-type material and the channel is n-type material, the polarity of the potential difference between the gate and source shown in Figure 6 would forward bias the p-n junction. However, remember that the gate is physically, and therefore electrically, insulated from the channel by the thin layer of silicon oxide so this is impossible.

The V_{GS}-I_{DS} transfer characteristic
Figure 7 below shows the graph of gate-source voltage versus drain-source current for an N-channel MOSFET.

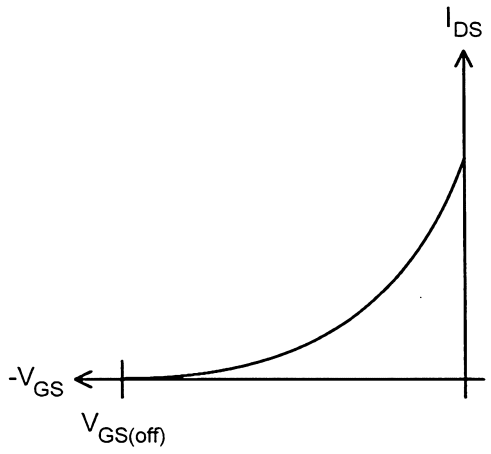

Figure 7 *The graph of negative gate-source voltage versus drain-source current for a depletion mode MOSFET*

This graph is basically the same as the V_{GS}-I_{DS} transfer characteristic for JFETs (see page 6-9 to compare). That being the case, depletion mode MOSFET biasing circuits, amplifier configurations and DC & AC calculations are all identical to those for JFETs.

Examples of depletion mode MOSFET circuits are shown below and overleaf.

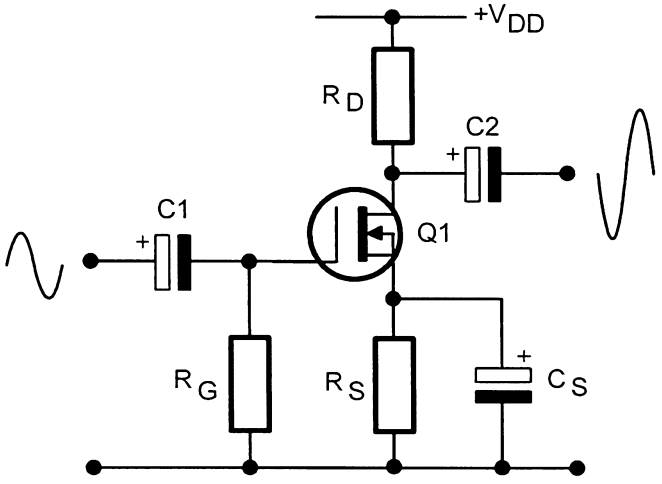

Figure 8 *Self biased, common source depletion mode MOSFET amplifier*

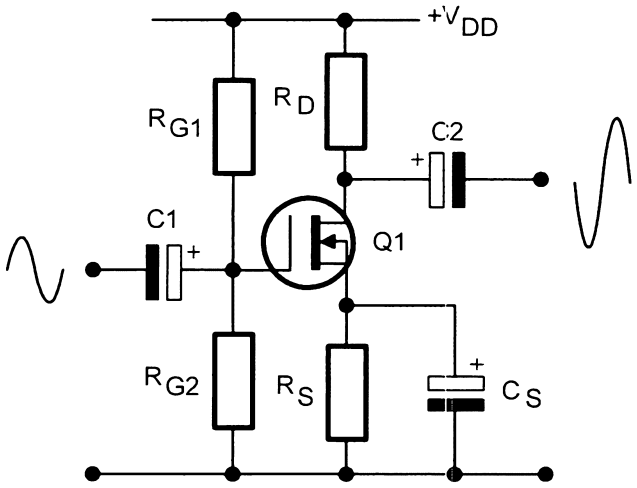

Figure 9 *Voltage divider biased, common source depletion mode MOSFET amplifier*

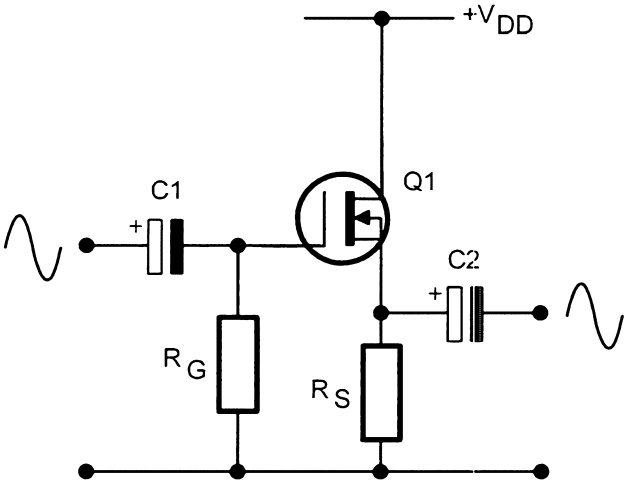

Figure 10 *Self biased, common drain depletion mode MOSFET amplifier*

Practise calculating the quiescent DC conditions and AC parameters of depletion mode MOSFET amplifiers by trying the following questions.

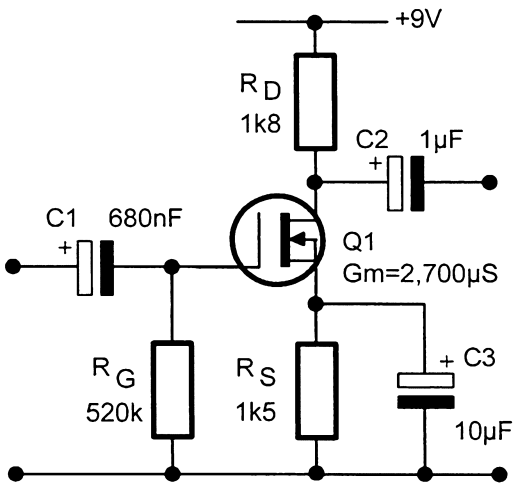

Figure 11

1. What is the gate voltage (V_G)?

2. Calculate the source voltage (V_S), given V_{GS} = -3V.

3. Calculate the drain-source current (I_{DS}).

4. Calculate the drain voltage (V_D).

5. Calculate the drain-source voltage (V_{DS}).

6. Determine the maximum peak-to-peak output voltage before clipping.

7. Calculate the unloaded voltage gain.

8. What is the input resistance?

9. What is the output resistance?

The enhancement effect in depletion mode MOSFETs

Although the graphs of gate-source voltage versus drain-source current for the MOSFET and JFET look similar (see pages 8-7 and 6-9 respectively), there is a big difference between them that must now be discussed.

Recall that N-channel JFETs are never operated so that the gate is made positive with respect to the source (or negative with respect to the source for a P-channel JFET). This is demonstrated using the transfer characteristic for an N-channel JFET in Figure 12 below.

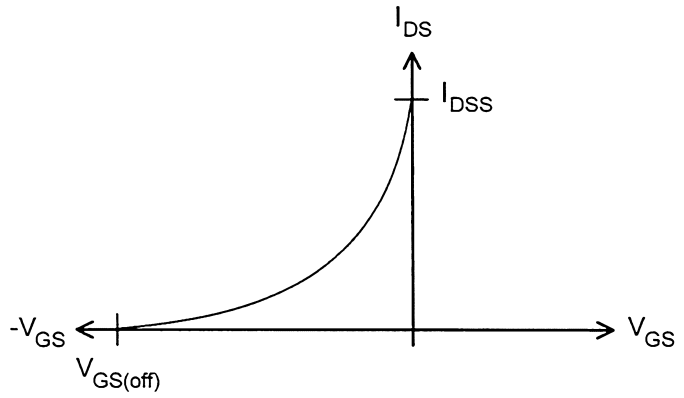

Figure 12 *The gate of an N-channel JFET is never made positive with respect to the source*

If the polarity of a JFET's normal operating gate-source voltage is reversed (for example, the gate of an N-channel JFET is made positive with respect to the source), the gate-source p-n junction would become forward biased. In the process, control over the drain-source current would be lost and a gate current would flow (either in or out depending on the type of JFET). The net effect is, the JFET would no-longer be operating as a transconductance amplifier.

However, a MOSFET's gate-source voltage can be reversed without upsetting its operation. To explain, the operation of the n-channel MOSFET discussed so far involves applying a potential difference across the gate and source that is the correct polarity for forward biasing the MOSFET's internal p-n junction. Of course, this doesn't happen because the gate is insulated.

That being the case, reversing the polarity of a MOSFET's gate-source voltage is the correct polarity for reverse biasing the MOSFET's internal p-n junction and so this is allowed and is shown in Figure 13 on the next page.

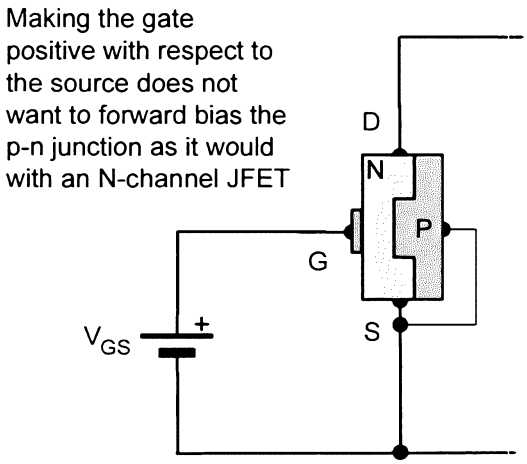
Making the gate positive with respect to the source does not want to forward bias the p-n junction as it would with an N-channel JFET
D
N
P
G
S
V_{GS}
+

Figure 13

Importantly, making the gate voltage positive with respect to the source attracts free electrons away from the depletion layer and into the channel. At the same time, free electrons in the p-type material would be attracted toward the p-n junction. This forces holes in the p-type material to move away from the p-n junction. These two reactions have the combined effect of making the depletion layer thinner and so the channel becomes more conductive. That being the case, the graph of gate-source voltage versus drain current for the depletion mode MOSFET actually looks like Figure 14 below.

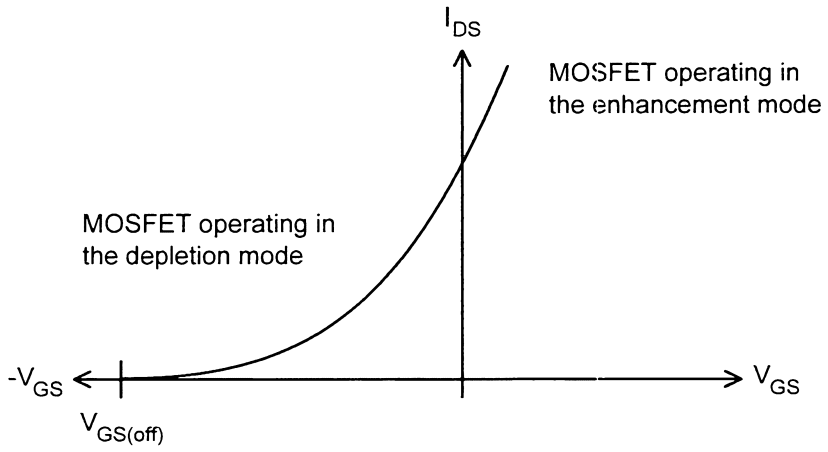

Figure 14 *The graph of gate-source voltage versus drain current for a depletion mode MOSFET*

When the gate-source voltage is made negative (for an N-channel MOSFET), the device is said to be operating in the *depletion mode* because the channel is depleted of carriers (free electrons for an N-channel MOSFET and holes for a P-channel MOSFET). But when the gate-source voltage is made positive, the device is said to be operating in the *enhancement mode* because the number of current carriers in the channel is enhanced. It is for this reason that depletion mode MOSFETs are also known as *depletion-enhancement mode* MOSFETs.

So, to summarise the full operation of the depletion mode MOSFET we can say the following things:

- If there is no potential difference between the gate and the source the MOSFET is neither in the depletion or enhancement mode. A "natural" level of depletion layer exists that affects the amount of drain-source current.

- If the gate is made negative with respect to the source for an N-channel MOSFET or positive with respect to the source for a P-channel MOSFET, the depletion layer gets bigger and so the drain-source current goes down. In this condition, the MOSFET is said to be operating in the depletion mode.

- If the gate is made positive with respect to the source for an N-channel MOSFET or negative with respect to the source for a P-channel MOSFET, the depletion layer gets smaller and so the drain-source current goes up. In this condition, the MOSFET is said to be operating in the enhancement mode.

As the depletion mode MOSFET can operate in both the depletion and enhancement modes, it is not necessary to ensure that the gate is biased so that it's quiescent DC voltage is negative with respect to the source for normal operation as must be done to JFETs. This means that the number of components needed in the self biased, common source amplifier can be reduced by removing the source resistor. Moreover, without the source resistor, the source resistor by-pass capacitor is also superfluous. These changes are shown in Figure 15 below.

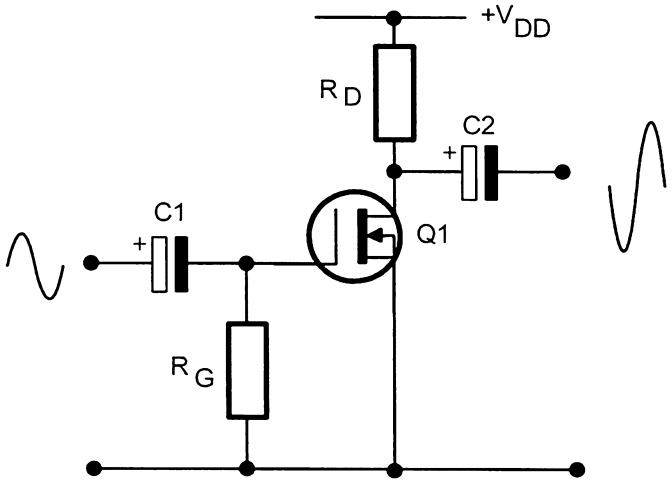

Figure 15 *Self biased, common source MOSFET amplifier that operates in both modes*

Like all other self biased FET amplifiers, the circuit has a gate voltage (V_G) of zero volts. And, because the source voltage (V_S) is also zero volts the gate-source voltage (V_{GS}) is zero volts. When the input signal goes positive, the gate becomes positive with respect to the source and the MOSFET is operated in enhancement mode. In which case, the drain current increases and V_D goes down. As the input signal goes negative, the gate becomes negative with respect to the source and the MOSFET is operated in depletion mode. In which case, the drain current drops and V_D goes up.

The DC and AC calculations are the same as for the self biased, common source MOSFET amplifier in Figure 8.

Practise analysing the quiescent DC conditions and AC parameters of this circuit by trying the following questions.

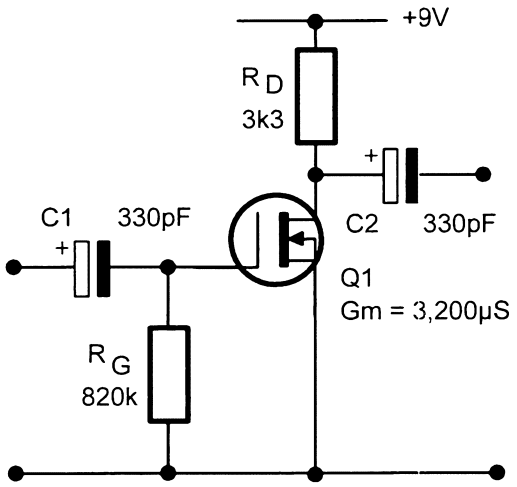

Figure 16

1. What is the gate voltage (V_G)?

2. What is the source voltage (V_S)?

3. Calculate the drain voltage (V_D), given V_{DS} is 5V.

4. Calculate the potential difference across the drain resistor (V_{RD}).

5. Calculate the drain-source current (I_{DS}).

6. Determine the maximum peak-to-peak output voltage before clipping.

7. Calculate the unloaded voltage gain.

8. What is the input resistance?

9. What is the output resistance?

Enhancement mode MOSFETs

The enhancement mode MOSFET is available in either N- or P-types but the physical construction is quite different to that of JFETs and depletion mode MOSFETs. Their schematic symbols and representative physical construction are shown in Figures 17 and 18. Like depletion mode MOSFETs and JFETs, the three terminals are called drain, gate and source.

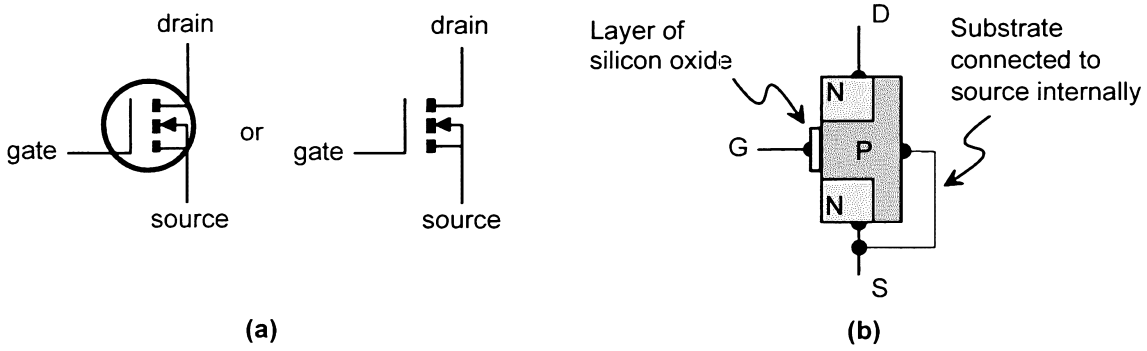

Figure 17 *(a) Schematic symbol of an N-type enhancement mode MOSFET; and (b) cross-sectional view of its construction*

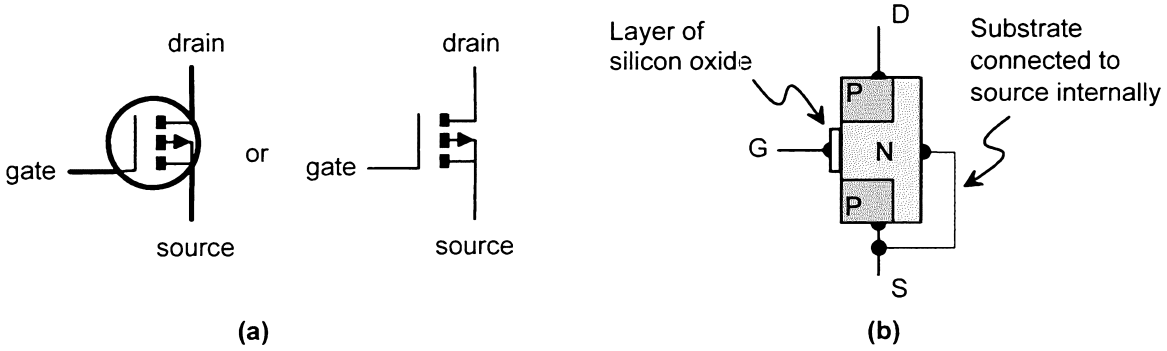

Figure 18 *(a) Schematic symbol of a P-type enhancement mode MOSFET; and (b) cross-sectional view of its construction*

The constructional diagram for each MOSFET shows why enhancement mode MOSFETs are called N-type or P-type and not N-channel or P-channel; there isn't a channel directly connecting the drain and the source. The schematic symbol represents this by using dashes between the drain and source instead of a line. You can use this information to remind you that the symbol is for the enhancement mode MOSFET and not the depletion mode MOSFET.

The gate of enhancement mode MOSFETs is still connected to the device by a very thin layer of silicon oxide (SiO_2). This means that enhancement mode MOSFETs have the very high input resistances of depletion mode MOSFETs and also demand the same level of handling care.

Enhancement mode MOSFET operation

It is useful to describe the operation of the enhancement mode MOSFET by comparing it to the BJT's operation. In fact, they're similar in several ways. Like the collector-emitter connection of a BJT, the drain-source connection is effectively an open-circuit. So, if a potential is applied between the drain and source no drain-source current (I_{DS}) flows (that is, with a gate-source voltage of zero). This is shown using an N-type enhancement mode MOSFET in Figure 19 below.

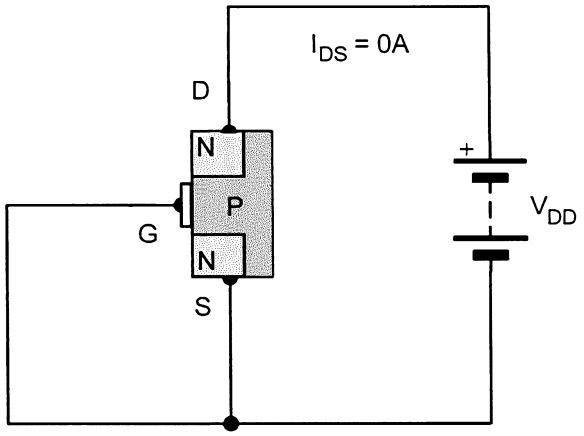

Figure 19 *No drain-source current flows in an enhancement mode MOSFET with V_{GS} = 0V*

This is the opposite to the normal operation of a JFET and depletion mode MOSFET. And, in fact, if the device is biased so that gate is made negative with respect to the source, drain-source current still wouldn't flow (which is also opposite to the normal operation of JFETs and depletion mode MOSFETs). To explain, consider the N-type enhancement mode MOSFET in Figure 20a. A depletion layer forms where the N-type and P-type materials touch. But, for reasons already explained, reverse biasing the gate-source connection makes the depletion layer bigger (see Figure 20b).

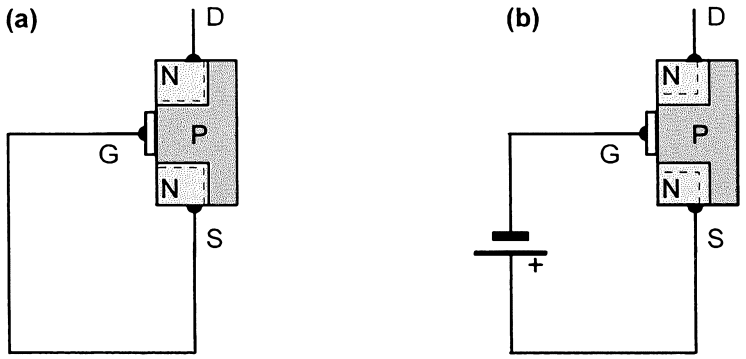

Figure 20 *(a) The "natural" depletion layer; and (b) the depletion layer effectively gets bigger if the gate is made negative with respect to the source*

However, if the gate of an N-type enhancement mode MOSFET is made positive with respect to the source (similar to making the base positive with respect to the emitter of an NPN BJT), for reasons already explained, the depletion layer gets thinner (see Figure 21a). If the gate voltage is made positive enough with respect to the source (typically 2V to 4V depending on the device) free electrons in the p-type material gather at the gate and form an artificial channel (see Figure 21b).

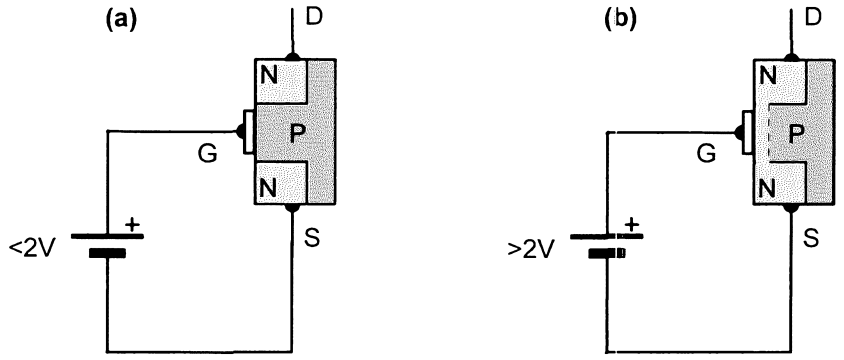

Figure 21 *(a) Making the gate positive with respect to the source effectively reduces the depletion layer; and (b) if the bias is made positive enough an artificial channel is formed*

When the artificial channel forms across the drain source connection, a drain-source current is able to flow (see Figure 22).

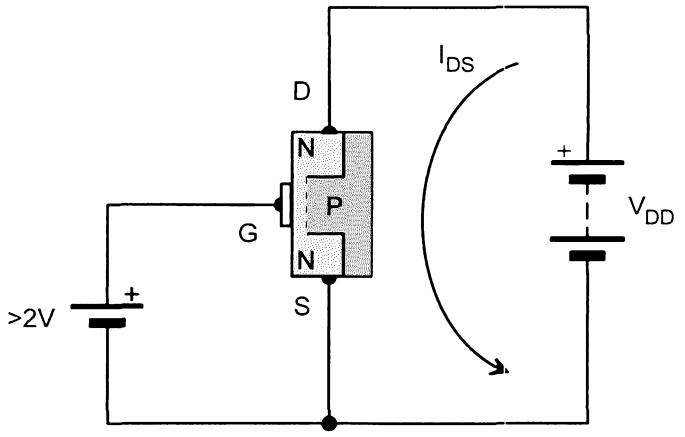

Figure 22 *When the gate is made positive enough with respect to the source a drain-source current flows*

The V_{GS}-I_{DS} transfer characteristic

Figure 23 below shows the graph of gate-source voltage versus drain-source current for an N-type enhancement mode MOSFET.

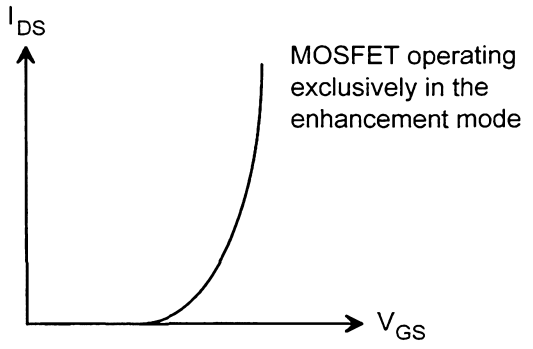

Figure 23 *Voltage-current curve for an enhancement mode MOSFET*

The graph shows that the enhancement mode MOSFET will only allow drain-source current to flow when the gate is made positive with respect to the source. In this way, the MOSFET operates like a BJT. The difference though is that, where a BJT needs between 0.5V and 0.7V to turn it on, the enhancement mode MOSFET needs a voltage more like 2V (but this will vary from device to device).

Enhancement mode MOSFET biasing circuits

Typical circuits used for enhancement mode MOSFETs include:

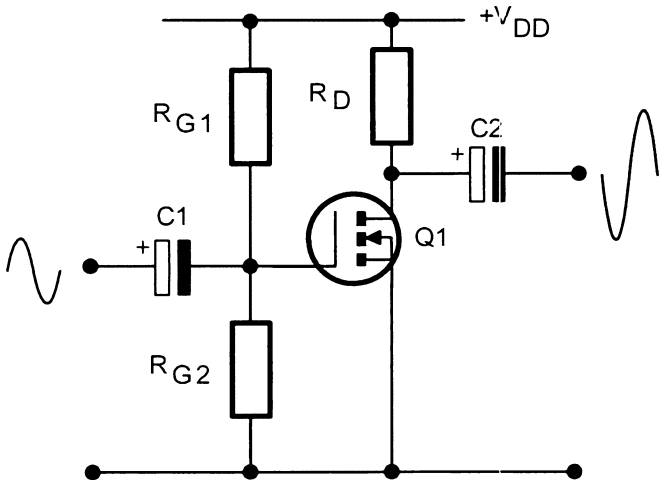

Figure 24 *Voltage divider biased, common source enhancement mode MOSFET amplifier*

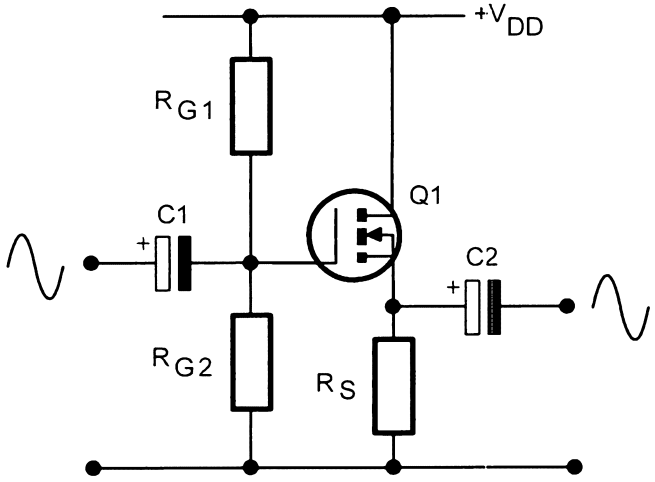

Figure 25 *Voltage divider biased, common drain enhancement mode MOSFET amplifier*

Notice that the circuits in Figures 24 and 25 use the voltage divider bias method and not self bias. The self bias circuit works for JFETs and depletion mode MOSFETs by making the gate negative with respect to the source which forces the FET into the depletion mode of operation. However, enhancement mode MOSFETs cannot operate in the depletion mode so the self bias circuit cannot be used.

DC and AC calculations

You're required to be able to calculate the voltages and currents around the circuit of enhancement mode MOSFET amplifier circuits (Figures 24 and 25). The appropriate equations can be found by looking at the equivalent circuits for depletion mode MOSFETs. As with other FET amplifier circuits you will be given one of the DC parameters with which to perform your calculations.

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Student notes

Skill practice 8

Practise measuring DC and AC voltages in MOSFET amplifiers using a DMM and an oscilloscope

This exercise is practise for the sorts of skills you may be required to perform in a practical test. Remember, in any practical tests you will be working alone so make sure that you can perform all the steps. It should take you about 1¼ hours to complete this exercise.

Equipment

- FET amplifier panel
- DMM
- three BNC to alligator-clip leads
- pin-to-pin leads
- banana leads

Remember:

Follow TAFE NSW WHS guidance at all times!

Work tasks

1. Read your WHS responsibilities at the top of the form below. Then conduct a WHS risk assessment and record your findings in the space provided.

Responsibilities of students under the Model WHS Act: s28

- Take reasonable care for your own health and safety by working safely at all times
- Take reasonable care to ensure that your acts or omissions don't put the health and safety of others at risk
- Follow all TAFE NSW WHS guidance and comply with all reasonable instructions from TAFE NSW staff to assist them in complying with the TAFE NSW WHS requirements
- In addition to the above, you must:
  - use and maintain machinery, tools and all other equipment properly and safely
  - ensure that your work area is free of hazards
  - notify a TAFE NSW staff member of actual or potential hazards
  - wear/use prescribed safety equipment
  - take notice of any safety signs and adhere to their instructions

Risks involved in this activity include:	**Control measures:**
Trip hazards (eg students bags) Objects dropped on feet (while equipment is taken to and from workbenches).	Move bags and other objects from walkways Plan lifting of equipment
Others: _____	Other: _____
_____	_____
_____	_____

My signature here indicates that I have read and understand my responsibilities under the Model WHS Act s28 (detailed above). I have also conducted a risk assessment before undertaking this activity and have identified measures to control these risks and have implemented them.

Signature: _____ Date: _____

2. Gather the equipment needed for this exercise.

3. Use the pin-to-pin leads to set up the circuit below on the FET amplifier panel.

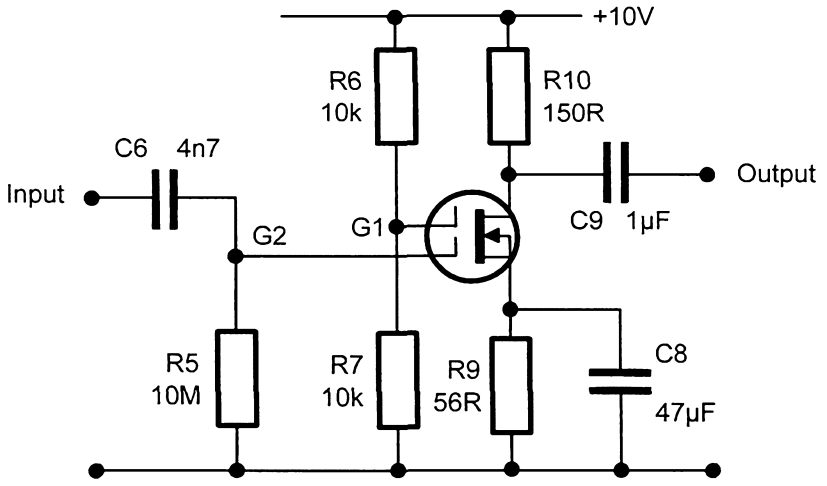

Figure 1

Notice that the MOSFET on this amplifier has two gates. These devices are common and are known as dual gate MOSFETs. Their operation is exactly the same as the single gate operation in terms of biasing requirements and so on.

Having two gates may seem like a serious complication but it's not. The effect of each gate on the FET's operation is the sum of the two gates. For example, if one gate was 1V DC and the other was 2V DC, the effect on the FET would be like having a single gate MOSFET with 3V DC on the gate.

So, lets have a quick look at the circuit of Figure 1. The "upper" gate (G1) is connected to a voltage divider so it will have some DC voltage on it but that's all. G2 is connected to ground via a 10M resistor so its DC voltage will be zero. However, any input signal applied to the circuit must be connected via this gate. Thus, the effect on the device of the two inputs is the same as an AC signal connected to a single gate MOSFET that has voltage divider biasing.

4. Adjust one of the bench-mounted DC power supply's outputs to 10V. Turn off the unit and connect it to the circuit.

5. Make sure all the fault switches are **OFF** and turn on the power supply.

6. Using the digital multimeter, measure the DC voltage on the BFR11's gate, source and drain with respect to common. Record these in Table 1 below.

7. Measure the gate-source voltage of the two gates. Record these in Table 1 also.

Table 1

V_{G1}	V_{G2}	V_D	V_s	V_{G1S}	V_{G2S}

Question 1
In what mode does the gate$_{(1)}$-source voltage (V_{G1S}) suggest the MOSFET is operating in?

☐ Depletion
☐ Enhancement

Question 2
In what mode does the gate$_{(2)}$-source voltage (V_{G2S}) suggest the MOSFET is operating in?

☐ Depletion
☐ Enhancement

Question 3
What is the input resistance for V_{G1}?

_____

Question 4
What is the input resistance for V_{G2}?

_____

The teacher needs to check your work at this point...

8. Connect a 1kHz 500mVp-p sinewave to the amplifier's input.

9. Check the signal at the output using the CRO to see whether or not it is clipped. If it is, gradually reduce the input voltage until the clipping is gone.

10. Measure the output voltage and calculate the gain. Record this information in Table 2 below.

Table 2

Vin	Vout	Av

Question 5
What is the phase relationship between the amplifier's input and output signals?

11. Measure the *f1* and *f2* points of the circuit. Record these values in Table 3 below.

Table 3

f1	f2

The teacher needs to check your work at this point...

12. Turn off the power supply and disconnect the signal generator from the panel.

13. Modify the circuit so that the drain resistor is 330Ω (see Figure 2).

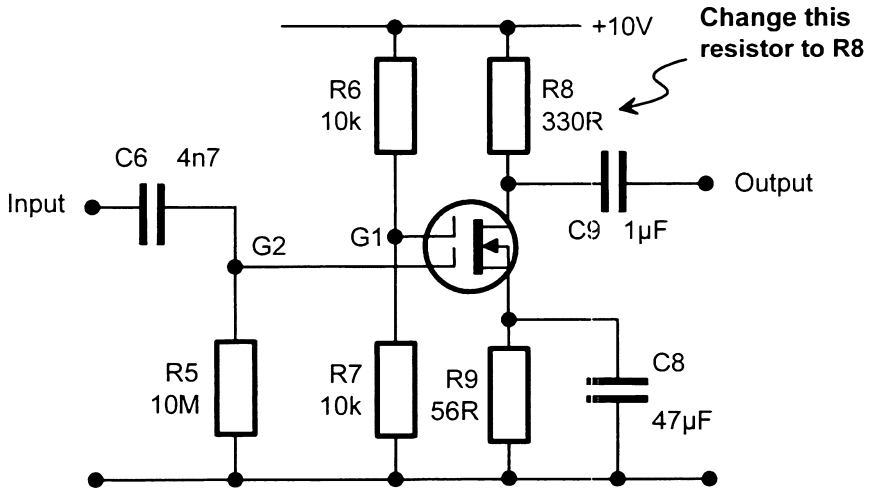

Figure 2

14. Turn on the power supply but don't reconnect the signal generator yet.

15. Measure the DC voltage on the BFR11's gate, source and drain with respect to common. Record these in Table 4.

16. Measure and record the gate-source voltage of the two gates. Record these in Table 4 also.

Table 4

V_{G1}	V_{G2}	V_D	V_s	V_{G1S}	V_{G2S}

Question 6
Is the voltage on the drain lower or higher that the voltage on the drain of the first circuit?

Question 7
What effect will having a lower V_D have on the performance of the circuit?

The teacher needs to check your work at this point...

17. Connect a 1kHz 500mVp-p sinewave to the amplifier's input.

18. Check the signal at the output to see whether or not it is clipped. If it is, slowly reduce the input voltage until the clipping is gone.

19. Measure the output voltage and calculate the gain. Record this information in Table 5 below.

Table 5

Vin	Vout	Av

Question 8
Why is the gain of this circuit different to the gain of the first circuit?

The teacher needs to check your work at this point...

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Student notes

Review questions

Answer these questions to check your understanding of what you have learnt for this chapter. Doing this will also help to prepare you for the tests.

1. What is an advantage and a disadvantage of the insulated gate of MOSFETs over BJTs?

_____

_____

2. In what mode or modes of operation can an n-channel depletion MOSFET operate?

- ☐ Depletion mode only
- ☐ Both depletion and enhancement modes
- ☐ Enhancement mode only
- ☐ Universal mode

3. Which bias allows drain-source current to flow in a depletion mode MOSFET?

- ☐ Only a gate-source voltage of 0V
- ☐ The gate voltage must be positive with respect to the source but not negative
- ☐ The gate voltage must be negative with respect to the source but not positive
- ☐ The gate voltage can be either positive or negative with respect to the source

4. In what mode or modes of operation can an n-type enhancement MOSFET operate?

- ☐ Depletion mode only
- ☐ Both depletion and enhancement modes
- ☐ Enhancement mode only
- ☐ Universal mode

5. Which bias allows drain-source current to flow in an n-type enhancement mode MOSFET?

- ☐ Only a gate-source voltage of 0V
- ☐ The gate voltage must be positive with respect to the source but not negative
- ☐ The gate voltage must be negative with respect to the source but not positive
- ☐ The gate voltage can be either positive or negative with respect to the source

Questions 6 and 7 refer to the circuit in Figure 1

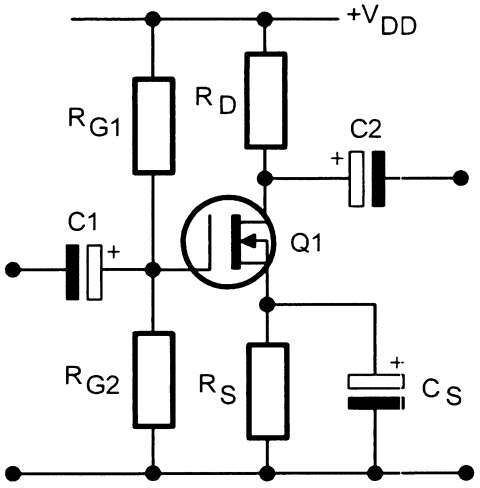

Figure 1

6. State the component that performs the functions listed below.

   (a) Converts changes in V_{GS} to changes in I_{DS} _____

   (b) Converts changes in I_{DS} to changes in V_D _____

   (c) Couples the output signal to the load _____

   (d) Stops the signal source affecting the DC gate voltage _____

   (e) By-passes the source resistor to increase the gain _____

   (f) Develops a source voltage and provides DC feedback _____

7. Must the voltage on the MOSFET's gate be positive or negative with respect to the source, or can it be either? Explain your answer.

   _____

   _____

   _____

Questions 8 to 22 refer to the circuit in Figure 2

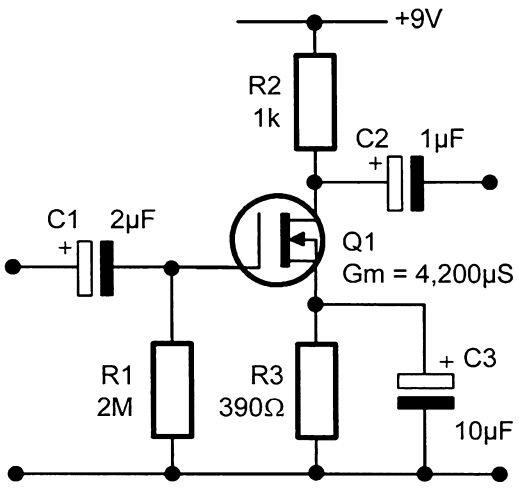

Figure 2

8. What is the gate voltage (V_G)?

9. Calculate the source voltage (V_S) given V_{GS} is -1.5V.

10. Calculate the drain voltage (V_D).

11. Calculate the drain-source voltage (V_{DS}).

12. Determine the maximum peak-to-peak output voltage before clipping.

13. What biasing method does the circuit use?

14. What configuration is the circuit?

15. What is the amplifier's input-output phase relationship?

16. Calculate the unloaded voltage gain.

17. What is the input resistance?

18. What is the output resistance?

19. Calculate the maximum peak-to-peak input signal before clipping of the output.

20. What would happen to the gain of the circuit if the capacitor *C3* became an open-circuit?

21. What is the purpose of *C1* and *C2*?

22. What would be the amplifier's new gain if a 680Ω load was connected across its output?

Questions 23 to 29 refer to the circuit in Figure 3

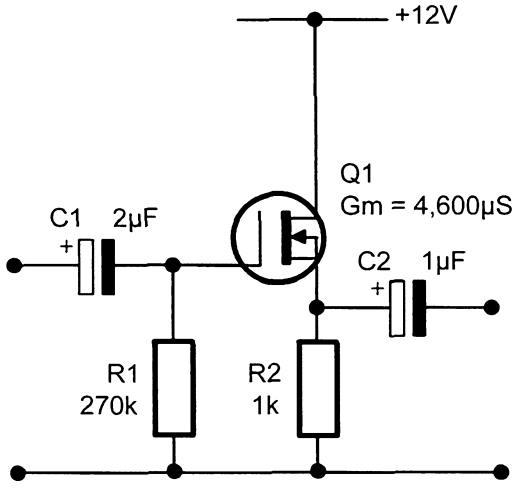

Figure 3

23. What biasing method does the circuit use?

24. What configuration is the circuit?

25. What is the amplifier's input-output phase relationship?

26. Calculate the unloaded voltage gain.

27. What is the input resistance?

28. Calculate the approximate output resistance.

29. Why wont the gain of this circuit change much when a load is connected?

30. What mode would the MOSFET in Figure 4 below be operating in during each half cycle of the input signal shown?

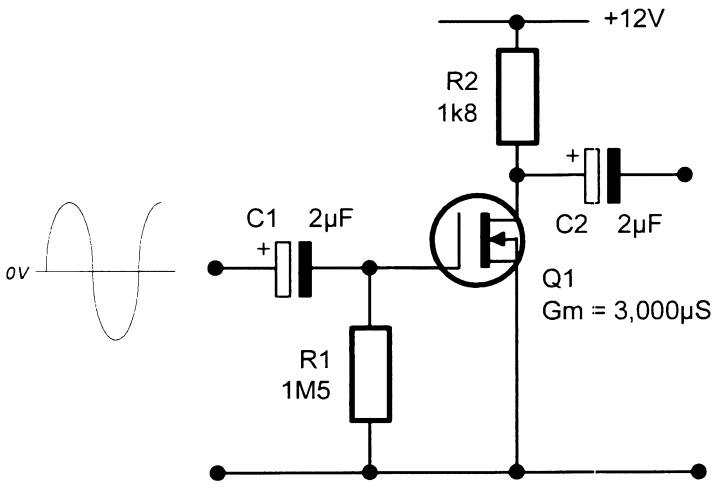

Figure 4

Questions 31 to 41 refer to the circuit in Figure 5 below

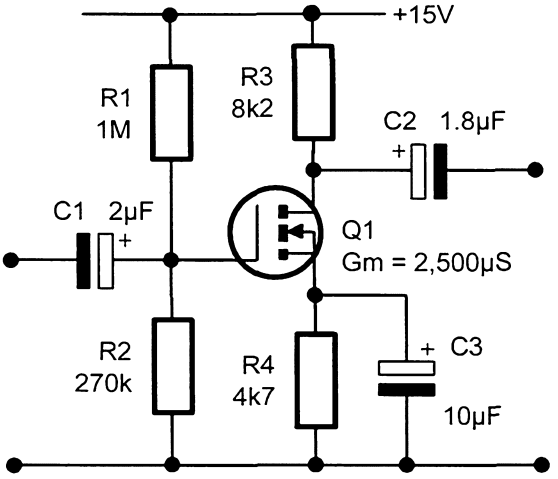

Figure 5

31. Calculate the gate voltage (V_G).

32. Calculate the source voltage (V_S) given V_{GS} is -1.8V.

33. Calculate the drain voltage (V_D).

34. Determine the maximum peak-to-peak output voltage before clipping.

35. What biasing method does the circuit use?

36. What configuration is the circuit?

37. What is the amplifier's input-output phase relationship?

38. Calculate the unloaded voltage gain.

39. Calculate the input resistance.

40. What is the output resistance?

41. Calculate the maximum peak-to-peak input signal before clipping of the output.

Questions 42 to 47 refer to the circuit in Figure 6

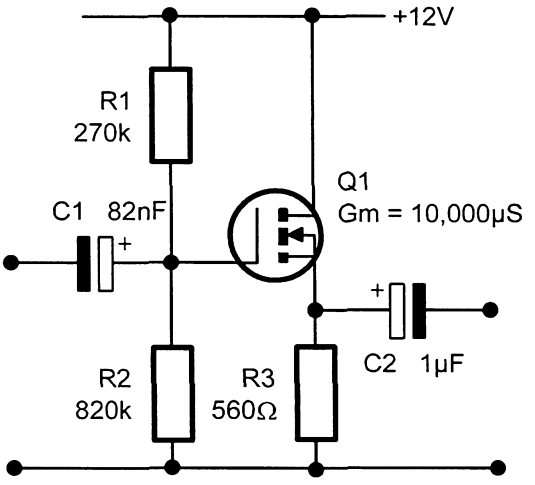

Figure 6

42. What biasing method does the circuit use?

43. What configuration is the circuit?

44. What is the amplifier's input-output phase relationship?

45. Calculate the unloaded voltage gain.

46. What would happen to the circuit if *R1* became faulty and went open-circuit?

47. What is likely to happen to the signal at the amplifier's output if the input signal is increased to 15Vp-p?

Appendix 1

Other base bias and voltage divider bias circuits

The BJT biasing circuits in Section 2 only show NPN BJTs in circuits with a positive supply and PNP BJTs in circuits with a negative supply. However, it's common to use these devices in biasing circuits that use the other polarity supply. That is, NPN BJTs can be used in circuits with a negative supply and PNP BJTs can be used in circuits with a positive supply.

Unfortunately, despite the wide use of these circuits, the time allocated to this subject is not enough to cover them as well as the rest of the required content. So, these notes have been provided for your information and it is highly recommended that you read through them at some stage.

Base bias

Figure 1 below shows a base biased NPN BJT amplifier with a negative supply.

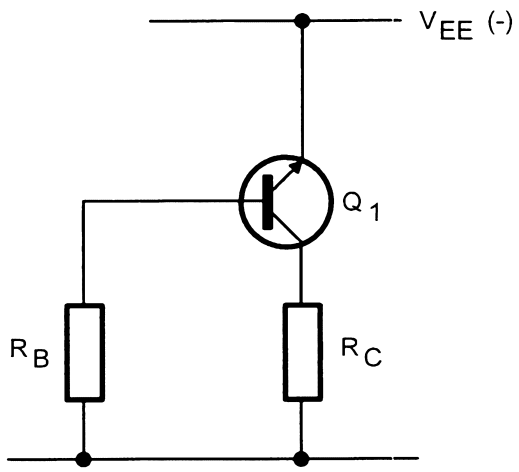

Figure 1 *A base biased NPN BJT amplifier with a negative supply*

At first glance the circuit might look strange. However, the conditions necessary to bias the NPN BJT are satisfied. As the emitter is connected to the supply, it has the most negative voltage on it. Or, put another way, the emitter is least positive. There is also a path for quiescent base current to (flow from common, into the base and towards the supply). And, the resulting collector current develops a potential difference across the collector resistor making the collector voltage the least negative or the most positive voltage in the circuit (assuming the value of R_C is appropriate).

It may be a little easier to see that the NPN BJT's biasing needs are satisfied by redrawing the circuit as shown in Figure 2 below. The currents in the circuit are shown as well as typical voltages around the circuit for a -9V supply rail. Notice that the BJT's base is still 0.6V more positive than the emitter.

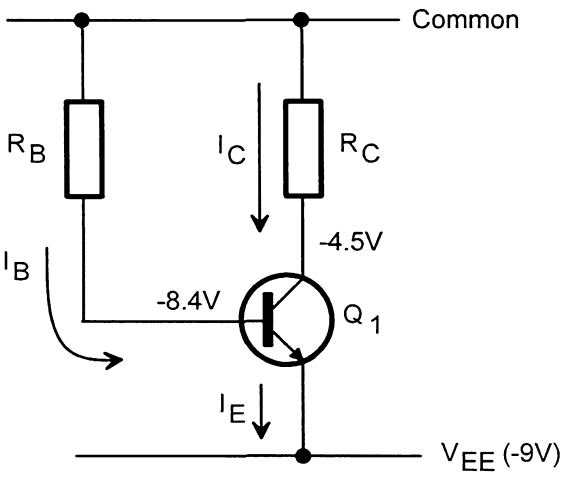

Figure 2 *The circuit in Figure 1 redrawn (with typical voltages added)*

Figure 3 below shows a base biased PNP BJT amplifier with a positive supply. Again, the currents are shown as well as typical voltages around the circuit for a 16V supply rail. Notice that the BJT's base is still 0.6V less positive than the emitter.

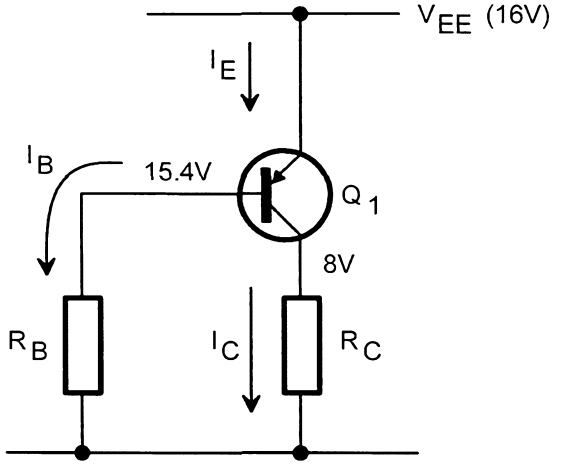

Figure 3 *A base biased PNP BJT amplifier with a positive supply*

The procedure for calculating the key circuit voltages is identical to the procedure in Section 2. However, Ohm's Law and Kirchhoff's Voltage Law dictate that two of the equations are different.

Find V_E As the emitter is directly connected to the supply rail then:

$$V_E = V_{EE}$$

Find V_B Recall that the connection between the base and the emitter of a BJT is a p-n junction. Recall also that, when a p-n junction is forward biased, its potential difference is 0.6V. And, as the emitter is connected to the supply rail, then:

$$V_B = V_{EE} - 0.6V \quad \text{for NPN}$$

$$V_B = V_{EE} + 0.6V \quad \text{for PNP}$$

Calculating the collector voltage is a three-step process:

1. Find I_B The base current is set by the base resistor and is found by dividing the potential difference across the resistor by its resistance (Ohm's Law). As the voltage on the BJT's base is the same as the voltage across R_B the base current can be found using the equation:

$$I_B = \frac{V_B}{R_B}$$

2. Find I_C Recall that the collector current is bigger than the base current by a factor of beta.

$$I_C = \beta \times I_B$$

3. Find V_C As the voltage on the BJT's collector is the same as the voltage across R_C the collector current can be found using the equation:

$$V_C = I_C \times R_C$$

Practise calculating the voltages around the circuit of a base biased NPN BJT using a negative supply by trying the following questions.

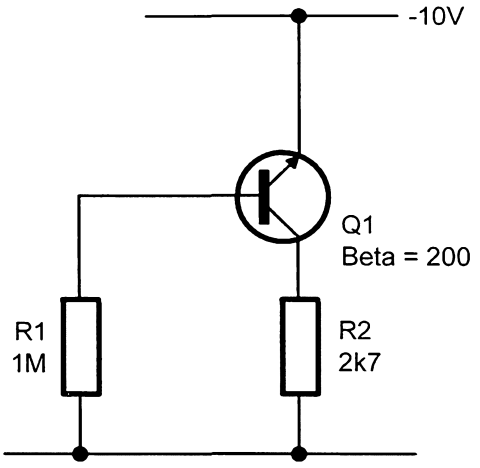

Figure 4

1. Calculate the base voltage (V_B) for the circuit in Figure 4.

2. Calculate the base current (I_B).

3. Calculate the collector current (I_C).

4. Calculate the collector voltage (V_C).

Voltage divider bias

Figure 5 below shows a voltage divider biased NPN BJT amplifier with a negative supply. Typical circuit voltages have been shown for a -12V supply.

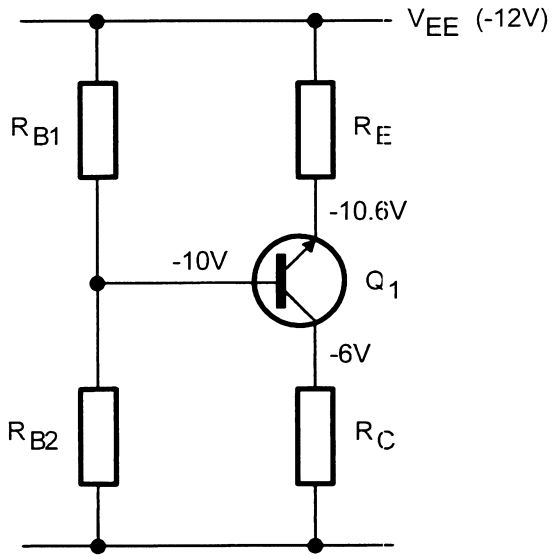

Figure 5 *A voltage divider biased NPN BJT amplifier with a negative supply*

Figure 6 below shows a voltage divider biased PNP BJT amplifier with a positive supply. Typical circuit voltages have been shown for a +10V supply.

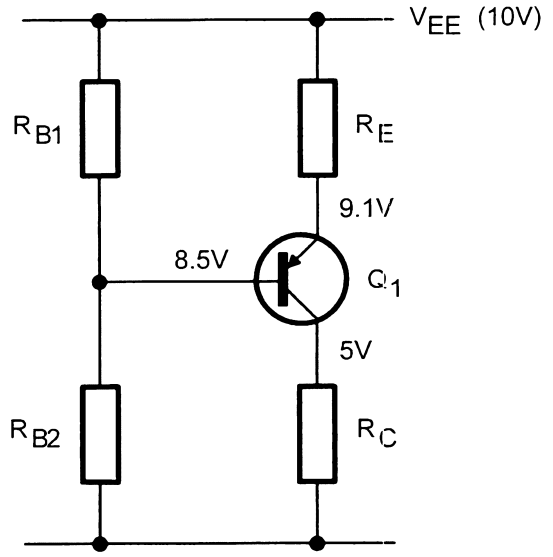

Figure 6 *A voltage divider biased PNP BJT amplifier with a positive supply*

Calculations

The procedure for calculating the key circuit voltages is identical to the procedure in Section 2. However, Ohm's Law and Kirchhoff's Voltage Law dictate that two of the equations are different.

Find V_B The base voltage is still found by using the voltage divider equation:

$$V_B = V_{EE} \times \frac{R_{B2}}{R_{B1}+R_{B2}}$$

Then the emitter voltage can be calculated.

Find V_E As we know, there is a potential difference across the base-emitter junction of 0.6V when the BJT is forward biased. So the emitter voltage is:

$$V_E = V_B - 0.6V \quad \text{for NPN}$$

$$V_B = V_B + 0.6V \quad \text{for PNP}$$

Finally, once the emitter voltage is known, the collector voltage can be found and this is a two-step process:

1. Find I_C The collector current is virtually the same as the emitter current so it can be found by calculating the emitter current. Be careful though, you must subtract the emitter voltage (V_E) from the supply voltage to find the voltage across the emitter resistor (V_{RE}) before dividing it by R_E.

$$I_C \approx I_E = \frac{V_{EE}-V_E}{R_E}$$

2. Find V_C The collector voltage is found by simply using Ohm's Law.

$$V_C = I_C \times R_C$$

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Practise calculating the voltages around the circuit of a voltage divider biased PNP BJT operating with a positive supply by trying the following questions.

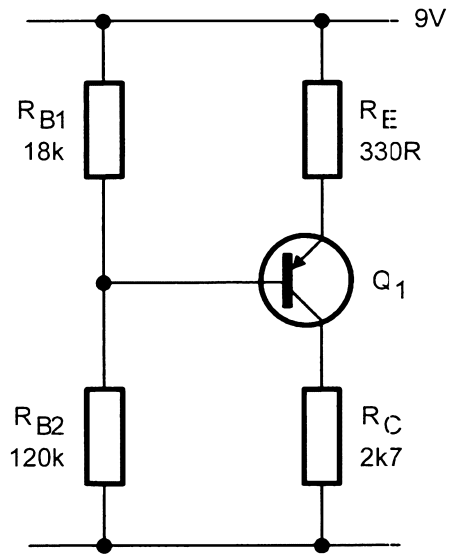

Figure 7

1. Calculate the base voltage (V_B) for the circuit in Figure 7.

2. Calculate the emitter voltage (V_E).

3. Calculate the collector current (I_C).

4. Calculate the collector voltage (V_C).

Appendix 2

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Section summaries

The theory notes in each Section of this workbook are designed to help you learn about the transistor amplifier circuits. But when you think about it, there's a difference between learning and remembering. These section summaries are designed to help you remember the theory.

Section 1

Objectives and Summary

1. Draw and identify the schematic symbols for NPN and PNP bipolar junction transistors (BJTs)

NPN PNP

2. Name the three terminals of a BJT

   See above.

3. State the bias conditions needed for the junctions of an NPN and PNP BJT for it to operate in amplifier circuits

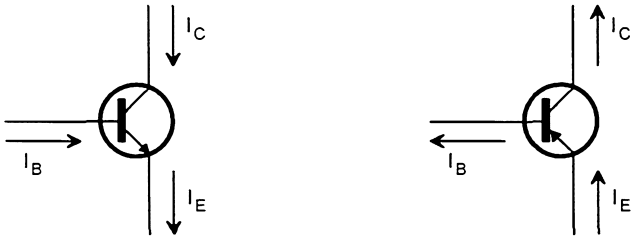
Junction	Condition
Collector-base	The C-B junction must be reverse biased.
Base-emitter	The B-E junction must be forward biased.

4. State the DC terminal requirements needed to obtain the junction bias conditions for an NPN and PNP BJT

NPN		
Terminal	**Label**	**Requirement**
Collector voltage (with respect to common)	V_C	This must be the most positive of the BJT's three terminals (eg +8V).
Base voltage (with respect to common)	V_B	This must be a voltage that is less positive than the collector's voltage (V_C) but at least 0.6V (eg +3V).
Emitter voltage (with respect to common)	V_E	This must be a voltage between 0V and the base voltage (V_B) (eg 2V).
Base-emitter voltage (with respect to emitter)	V_{BE}	This will range from between 0.5V and 0.7V for a forward biased NPN BJT.
Base current	I_B	There must be a path for a small current to flow from the *Vcc* into the base of the BJT.

PNP		
Terminal	**Label**	**Requirement**
Collector voltage (with respect to common)	V_C	This must be the most negative of the BJT's three terminals (eg -8V).
Base voltage (with respect to common)	V_B	This must be a voltage that is less negative than the collector's voltage (V_C) but at least 0.6V (eg -3V).
Emitter voltage (with respect to common)	V_E	This must be a voltage between 0V and the base voltage (V_B) (eg -2V).
Base-emitter voltage (with respect to emitter)	V_{BE}	This will range from between -0.5V and -0.7V for a forward biased PNP BJT.
Base current	I_B	There must be a path for a small current to flow out from the base of the BJT to the *Vcc*.

5. Show the direction of current flow at each terminal of an NPN and PNP BJT



6. Calculate either the base, emitter or collector currents of a BJT given values for two of the currents

   Use the review questions to practise this. The equation is:

   $I_E = I_B + I_C$

7. Explain the operating principles of a BJT

   The BJT is a current-controlled device. That is, collector current flows when there is a base current. Moreover, the amount of collector current is a function of the amount of base current. That is, as base current goes up, so does collector current.

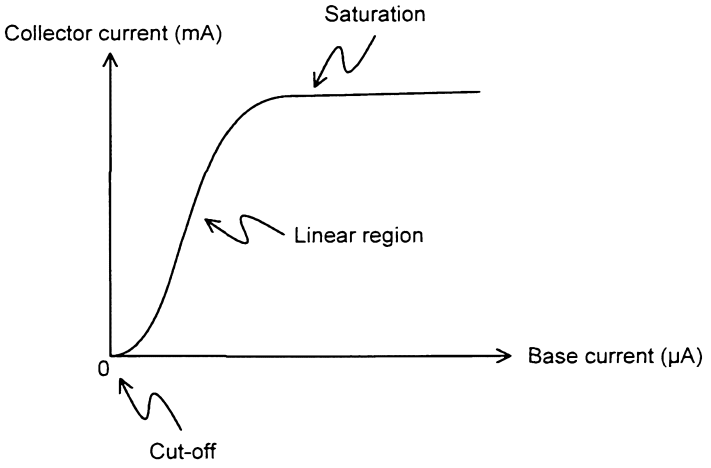
8. Define the terms *cut-off*, *linear operation* and *saturation* as applied to a BJT

   Cut-off is the condition of a BJT where the biasing is such that no current flows between its collector and emitter. In this condition, the BJT is said to be "turned off".

   Linear operation is the condition of a BJT where the biasing permits base current which in turn causes collector current. Importantly, if the base current varies, the collector current varies proportionally in response over a range of base currents. In this condition, the BJT is said to be "turned on".

   Saturation is the condition of a BJT where a practical maximum flows between its collector and emitter and so further increases in base current result in only small changes in collector current (relative to the BJT's linear region of operation). In this condition, the BJT is said to be "turned hard on".

9. Identify a BJT's cut-off, linear region and saturation region in a graph of base current versus collector current



10. Explain why a BJT is a current controlled device

    As already mentioned, it's the BJT's base current that causes collector current to flow. Moreover, if the base current varies, the collector current varies proportionally in response (assuming the BJT hasn't been driven into saturation).

11. Explain why a BJT is a current amplifying device

    As already mentioned, small base currents (typically in the μA for small signal transistors) cause the flow of relatively much larger collector currents (typically in the mA for small signal transistors). This is effectively current amplification.

12. Define the term *beta* as used with BJTs

    Beta is just a fancy name for current gain where the base current is said to be *Iin* and the collector current is said to be *Iout*.

13. Calculate either the beta, base current or collector current of a BJT given values for two of the quantities

    Use the review questions to practise this. The equation is:

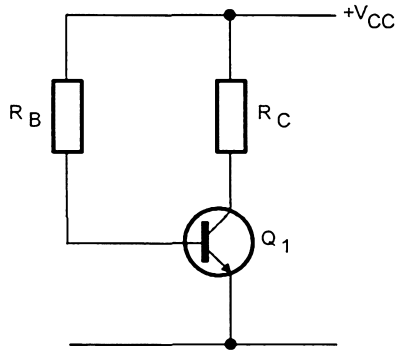
    $\beta = \frac{I_C}{I_B}$

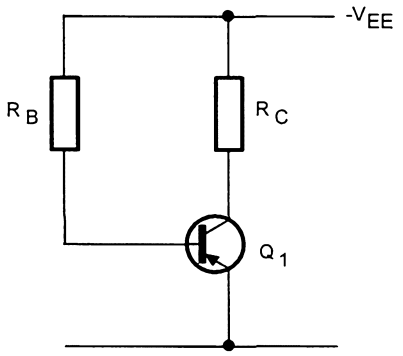
Section 2

Objectives and Summary

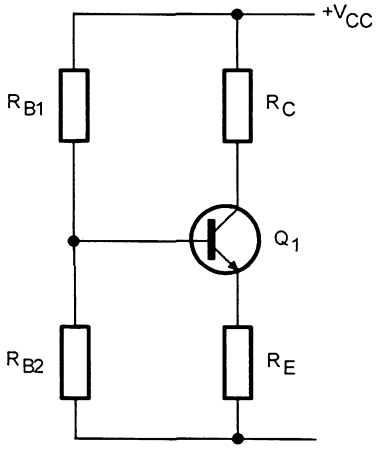
1. Recognise base biasing and voltage divider biasing BJT circuits in schematic diagrams

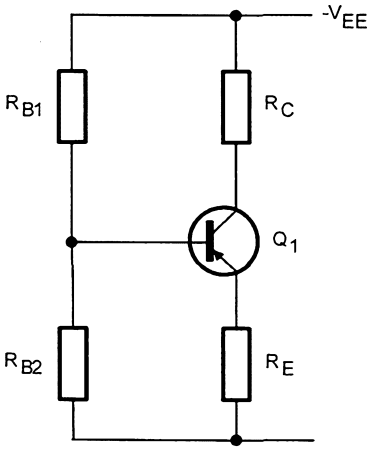
   Examples of base bias:





   Examples of voltage divider bias:





2. Explain the function of each component in the base bias and voltage divider bias circuits

Base bias:

R_B provides a path from the supply for base current to flow. At the same time, R_B sets the amount of base current that flows.

Q_1 amplifies the base current to produce a larger collector current.

R_B provides a path for the collector current to flow. It also sets up the quiescent DC collector voltage (V_C) and converts changes in collector current to changes in collector voltage.

Voltage divider bias:

R_{B1} **and** R_{B2} set up a fixed voltage on the base and provide a path from the supply for base current to flow.

Q_1 amplifies the base current to produce a larger collector current.

R_E sets the amount of emitter current (I_E) in the circuit. (It also provides negative feedback to the circuit.)

R_C provides a path for the collector current to flow. It also sets up the quiescent DC collector voltage (V_C) and converts changes in collector current to changes in collector voltage.

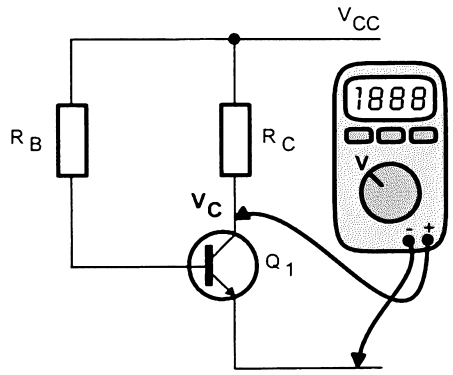
3. Predict key DC voltages around the base bias and voltage divider bias circuits

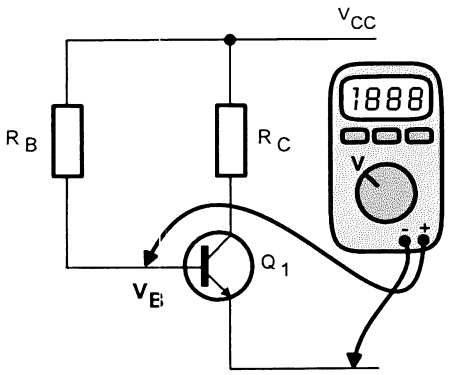
Base bias:	**Voltage divider bias:**
$V_B = 0.6V$ (NPN) $V_B = -0.6V$ (PNP)	$V_B = V_{CC} \times \frac{R_{B2}}{R_{B1}+R_{B2}}$
	$V_E = V_B - 0.6V$ $V_E = V_B + 0.6V$
$I_B = \frac{V_{CC}-V_B}{R_B}$	
$I_C = \beta \times I_B$	$I_C \approx I_E = \frac{V_E}{R_E}$
$V_{RC} = I_C \times R_C$	$V_{RC} = I_C \times R_C$
$V_C = V_{CC} - V_{RC}$	$V_C = V_{CC} - V_{RC}$
$V_{CE} = V_C - V_E$	$V_{CE} = V_C - V_E$
$V_{CB} = V_C - V_B$	$V_{CB} = V_C - V_B$

Note: Notice that the last four equations for the two biasing circuits are the same.

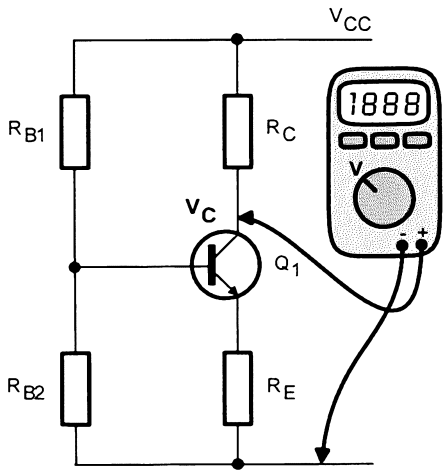
4. Measure key DC voltages around the base bias and voltage divider bias circuits and compare them to predicted values

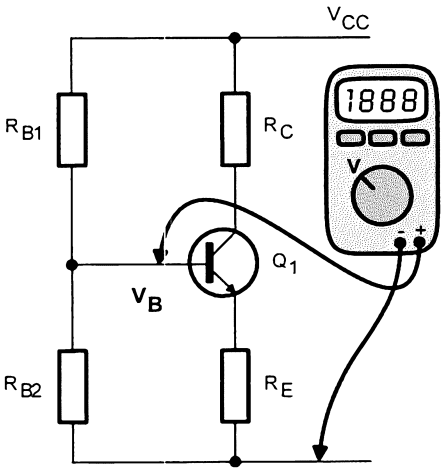
Base bias:

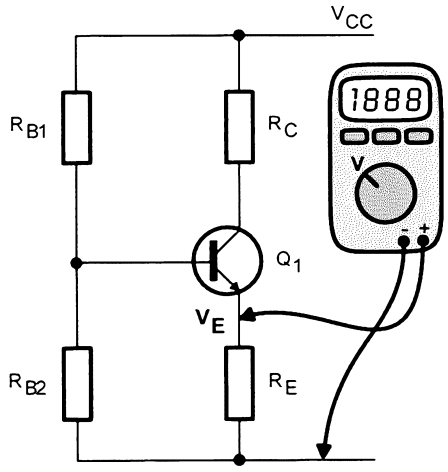




Voltage divider bias:







5. Explain why measured DC voltages are unlikely to be exactly the same as calculated values

Base bias:

i) Resistors have tolerances (typically ±5%)

ii) The forward voltage drop of the base-emitter junction is not exactly 0.6V

iii) The beta of BJTs varies from one to device to another

Voltage divider bias:

i) Resistors have tolerances (typically ±5%)

ii) The forward voltage drop of the base-emitter junction is not exactly 0.6V

[Notice that the variable beta of BJT's is not a factor for differences between calculated and measured voltages in voltage divider bias circuits. This is because the negative feedback introduced by R_E makes the circuit's gain largely independent of beta (as long as beta is large enough).]

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Section 3

Objectives and Summary

1. Identify the three BJT amplifier configurations

   To do this, look at the circuit's input and output connections. The configuration is called a "Common _____ " where the missing word is the same as the pin not being used for the signal's input and output. So:

   a) Input to base, output from collector so the circuit must be a Common Emitter
   b) Input to base, output from emitter so the circuit must be a Common Collector
   c) Input to emitter, output from collector so the circuit must be a Common Base

2. Identify the input and output terminals of each configuration

   Only two pins are used relative to common. Importantly...

   - Where the BJT's collector pin is used it is only ever as an output
   - Where the BJT's base pin is used it is only ever as an input
   - Where the BJT's emitter pin is used, it can be an input (CB) or an output (CC)

3. Describe the effects on the quiescent voltages and currents around the BJT configurations when an input signal is connected

Key

↑ means "goes up"
↓ means "goes down"
⇔ means "stays the same"

Common emitter (base bias):

As Vin ↑, V_{BE} ↑ (because V_E ⇔) so I_C ↑, which means V_{RC} ↑, and so V_C ↓
As Vin ↓, V_{BE} ↓ (because V_E ⇔) so I_C ↓, which means V_{RC} ↓, and so V_C ↑

Common emitter (voltage divider bias):

As Vin ↑, V_E ↑ (because V_{BE} ⇔) so I_E & I_C ↑, which means V_{RC} ↑, and so V_C ↓
As Vin ↓, V_E ↓ (because V_{BE} ⇔) so I_E & I_C ↓, which means V_{RC} ↓, and so V_C ↑

Common collector:

As Vin ↑, V_E ↑ by almost exactly the same amount (because V_{BE} ⇔)
As Vin ↓, V_E ↓ by almost exactly the same amount (because V_{BE} ⇔)

Common base:

As Vin ↑, V_E ↑ and so V_{BE} ↓ (because V_B ⇔) so I_C ↓, which means V_{RC} ↓, and so V_C ↑
As Vin ↓, V_E ↓ and so V_{BE} ↑ (because V_B ⇔) so I_C ↑, which means V_{RC} ↑, and so V_C ↓

4. State the signal input-output phase relationship for each configuration

	Common emitter	**Common collector**	**Common base**
Phase relationship	**Inverted**	In-phase	In-phase

5. List the main characteristics and applications of each configuration

Parameter	**Common emitter**	**Common collector**	**Common base**
Voltage gain	3 to 300	Slightly less than 1	Up to 300
Input resistance	Medium to high	Medium to high	Very low
Output resistance	Medium to high	Low	Medium to high
Main use	General purpose small signal amp	Buffer & Impedance matching	Amplify small signals in RF gear

6. State the two factors that determine the maximum peak-to-peak output voltage of a BJT amplifier

   - The size of the supply voltage
   - The quiescent DC voltage on the transistor's terminal that the output is taken from (either the collector or the emitter depending on the configuration)

   Note: The amount of loading affects this too but that's not an issue dealt with in the subject.

7. Calculate the maximum peak-to-peak output voltage of a BJT amplifier

   If the voltage on the output lead is less than half of the supply voltage then the maximum peak-to-peak output voltage is found using the equation:

   Common emitter: $Vout_{(max)} = V_C \times 2$

   Common collector: $Vout_{(max)} = V_E \times 2$

   If the voltage on the output lead is more than half of the supply voltage then the maximum peak-to-peak output voltage is found using the equation:

   Common emitter: $Vout_{(max)} = (V_{CC} - V_C) \times 2$

   Common collector: $Vout_{(max)} = (V_{CC} - V_E) \times 2$

   Note: This is an oversimplification and assumes the circuit is unloaded or lightly loaded.

   Once the maximum peak-to-peak output voltage before clipping is known, the maximum input voltage can be found using the equation:

   $$Vin_{(max)} = \frac{Vout_{(max)}}{Av}$$

8. Measure the gain, phase relationship and maximum peak-to-peak output voltage of a common emitter and common collector BJT amplifier

   See the Skill Practice Exercise.

Section 4

Objectives and Summary

1. Calculate (using approximation equations) the voltage gain, input resistance and output resistance of the common emitter BJT amplifier configuration

   Use the review questions to practise this. The equations are:

R_E un-by-passed	**R_E by-passed**
$r_e = \frac{26mV}{I_E}$	$r_e = \frac{26mV}{I_E}$
$Rin = R_{B1}//R_{B2}//\beta \times (R_E + r_e)$	$Rin = R_{B1}//R_{B2}//(\beta \times r_e)$
$Rout = R_C$	$Rout = R_C$
$Av_{(unloaded)} = \frac{R_C}{r_e+R_E}$	$Av_{(unloaded)} = \frac{R_C}{r_e}$
$Av_{(loaded)} = \frac{R_C//R_L}{r_e+R_E}$	$Av_{(loaded)} = \frac{R_C//R_L}{r_e}$

2. Calculate (using approximation equations) the voltage gain, input resistance and output resistance of the common collector BJT amplifier configuration

   Use the review questions to practise this. The equations are:

   $r_e = \frac{26mV}{I_E}$

   $Rin = R_{B1}//R_{B2}//\beta \times (R_E + r_e)$

   $Rout \approx r_e$

   $Av_{(unloaded)} = \frac{R_E}{r_e+R_E}$

   Note: It's possible to load the common collector BJT amplifier configuration but that's not applicable to the calculations in the Part 1 workbook.

3. Measure the unloaded and loaded voltage gain of the common emitter and common collector BJT amplifier configurations

   See the Skill Practice Exercise.

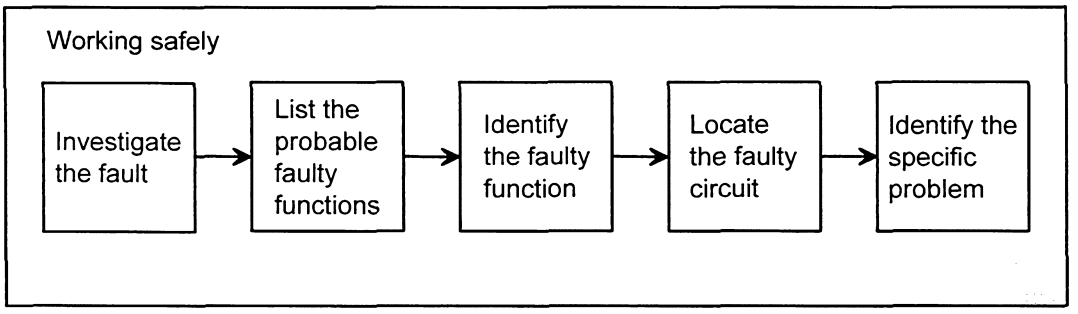
4. Measure the frequency response of BJT amplifiers

   See the Skill Practice Exercise.

Section 5

Objectives and Summary

1. List the five steps in the complete fault-finding process



2. Briefly describe each step in the complete fault-finding process

   The first step involves obtaining as much information about the fault as possible by consulting the customer and operating the equipment in as many modes of its operation as possible (or practical) to see what symptoms change or disappear (if any) and what new symptoms appear (if any).

   As its name implies, the second step involves making a list of the system *functions* that, if faulty in some way, could cause some or all the observed symptoms.

   The third step involves testing the probable faulty functions by taking measurements with a DMM or CRO (or by some other means) to identify which one (or ones) are actually faulty.

   The fourth step involves using techniques like signal tracing (and others) to locate the circuit within the function that is causing the problem.

   The fifth step involves making the necessary checks and/or measurements around the faulty circuit to identify the specific problem (it may not be a failed component).

3. List the changes to AC signals around BJT amplifiers that indicate the presence of a fault

   - Output signal too small
   - Output signal too big
   - No output signal at all
   - Output signal clipped (when it shouldn't be for the size of the input signal)
   - Output signal distorted in some other way

4. Predict the effect on the quiescent DC voltages of a BJT amplifier circuit for a given fault

   It's not recommended that you memorise the notes on pages 5-6 to 5-8 to satisfy this objective because there are too many possible faults. You're much better off making sure that you really understand how the DC quiescent conditions around voltage divider biased circuits are affected by one another. Then think about possible component faults and think about how they would affect the DC quiescent conditions.

5. Identify the specific problem in a faulty a BJT amplifier circuit

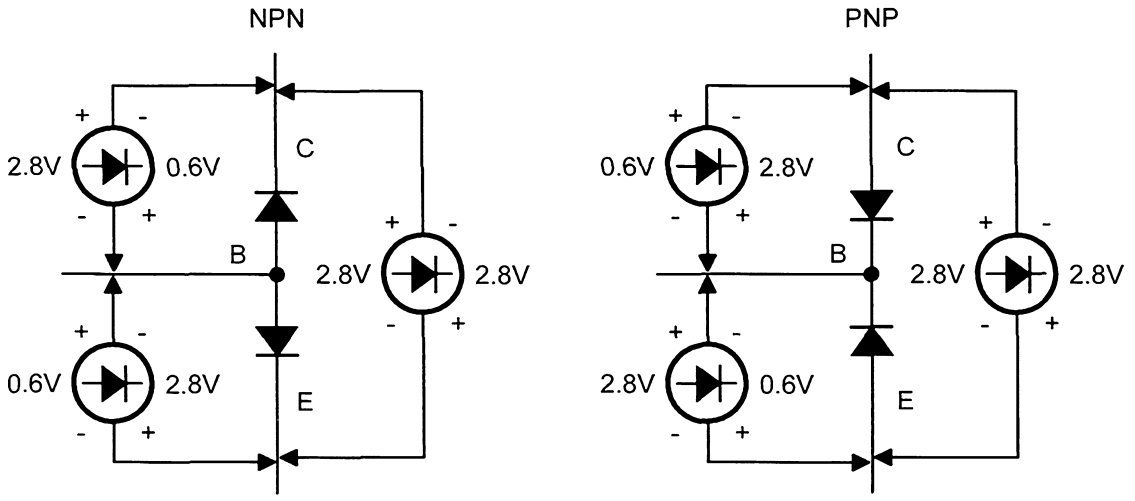
   Again, it's not recommended that you memorise the notes on pages 5-6 to 5-8 to satisfy this objective (or the list below for that matter which is not complete anyway). The following are some examples to get you started...

	V_B	V_E	V_C	Fault
1	High	High	Low	R_{B1} has gone low (unlikely) or R_{B2} has gone high (likely)
2	Low	Low	High	R_{B1} has gone high (likely) or R_{B2} has gone low (unlikely)
3	NC	NC	High	R_E has gone high (likely) or R_C has gone low (unlikely)
4	NC	NC	Low	R_E has gone low (unlikely) or R_C has gone high (likely)
5	Low	V_B	Vcc	Base-emitter short-circuit
6	NC	NC	Vcc	Collector open-circuit
7	NC	0V	Vcc	Emitter (or base) open-circuit
8	NC	V_C	V_E	Collector-emitter short-circuit
9	0V	0V	Vcc	R_{B1} open-circuit
10	NC	NC	Floats	R_C open-circuit

Key: NC = No Change
High = Voltage is higher than it should be
Low = Voltage is lower than it should be
V_{CC} = Voltage equal to the supply voltage

6. Test BJTs for faults using a digital multimeter

The readings that you should get for a working NPN and PNP transistor when tested on the diode test most of a typical DMM are shown below. If you get something other than this, the device is probably faulty.



7. Use manufacturers' data sheets to look up relevant DC terminal characteristics of BJTs

When you look-up BJT data sheets, the main performance characteristics that you are likely to need to look for include:

- Package (or case)
- Pinout
- NPN or PNP
- V_{CE} (maximum rating)
- V_{CB} (maximum rating)
- I_C
- Power rating
- Beta (also known as h_{FE})
- F_T

8. Choose a replacement BJT using manufacturers' data

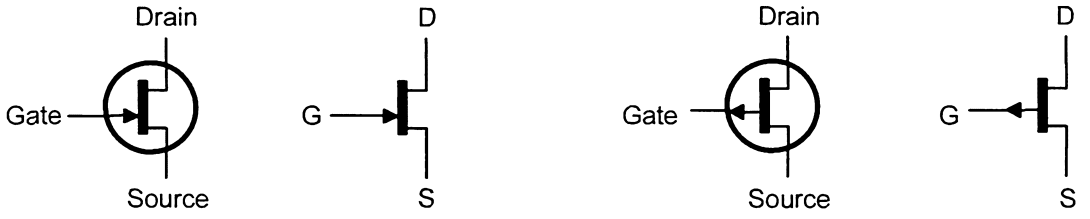
In the following order, choose a replacement BJT that:

- Is same type as the original (that is, replace NPN with NPN and PNP with PNP)
- Is made using the same semiconductor material as the original (that is, replace silicon with silicon and germanium with germanium)
- Has ratings for the following electrical specifications that are equal to, or better than, the original: $V_{CE(max)}$; $I_{C(max)}$; $P_{(max)}$; and $V_{CB(max)}$.
- Has the same package (or case) as the original
- Has the same pinout as the original
- Has approximately the same range of betas as the original
- Has a switching speed equal to, or better than, the original

Section 6

Objectives and Summary

1. Draw and identify the schematic symbols for N-channel and P-channel JFETs



N-channel **P-channel**

2. Name the three terminals of a JFET

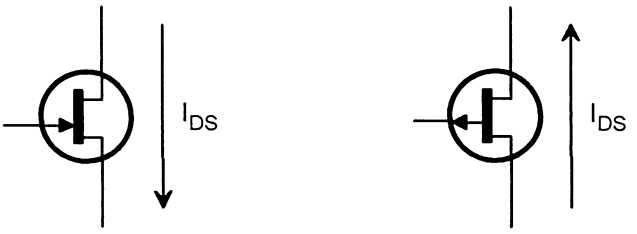
   See above.

3. Describe the bias conditions needed for each junction of a JFET for it to operate in amplifier circuits

   N-channel: Drain must be the most positive of the three terminals, then the source, then the gate.

   P-channel: Drain must be the most negative of the three terminals, then the source, then the gate.

4. Show the direction of current flow at each terminal of the JFET



Note: No current flows either in or out of the gate.

5. Explain the operating principles of JFETs

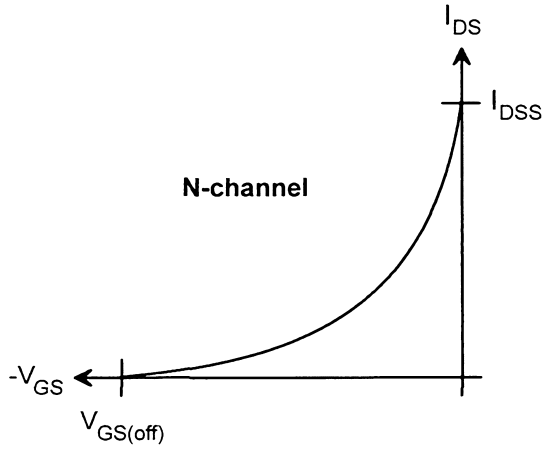
The JFET is a voltage-controlled device. That is, drain-source current flows when:

- there is a negative potential difference between the gate and the source ($-V_{GS}$) for the N-channel JFET.
- there is a positive potential difference between the gate and the source (V_{GS}) for the P-channel JFET.

Moreover, the amount of drain current is a function of the size of gate-source voltage. That is:

- as $-V_{GS}$ increases drain current goes down for the N-channel JFET.
- as V_{GS} increases, drain current goes down for the P-channel JFET.

6. Interpret graphs for JFET input-output transfer characteristics

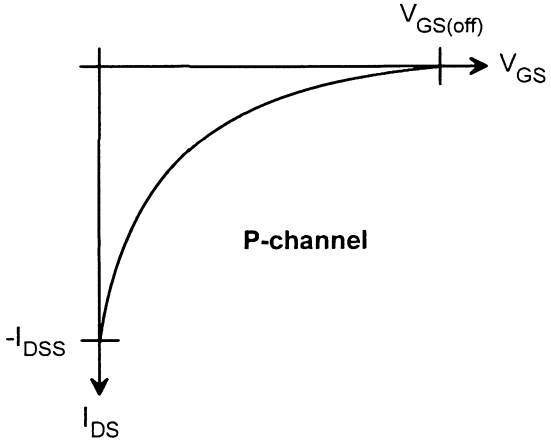


This graph tells us three things:

i) When the gate and source voltages are the same, maximum or "saturation" drain-source current (I_{DSS}) flows.

ii) As the gate voltage becomes more negative relative to the source voltage, the drain-source current (I_{DS}) goes down.

iii) When the gate voltage is sufficiently negative relative to the source, the drain-source current (I_{DS}) is zero.



This graph tells us three things:

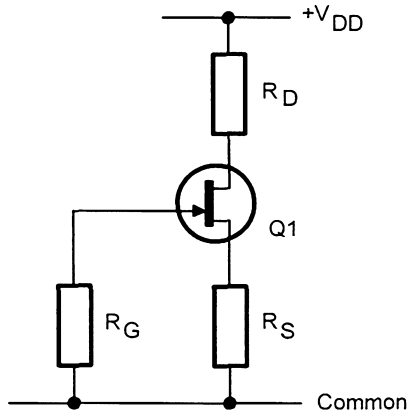
i) When the gate and source voltages are the same, maximum or "saturation" drain-source current (I_{DSS}) flows.

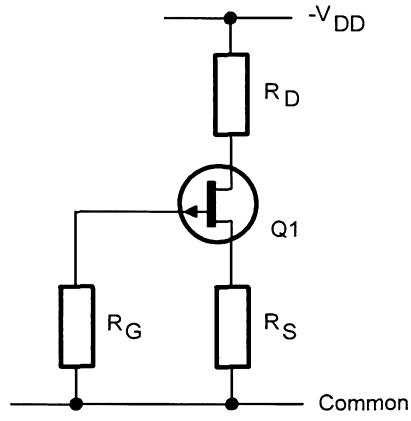
ii) As the gate voltage becomes more positive relative to the source voltage, the drain-source current (I_{DS}) goes down.

iii) When the gate voltage is sufficiently positive relative to the source, the drain-source current (I_{DS}) is zero.

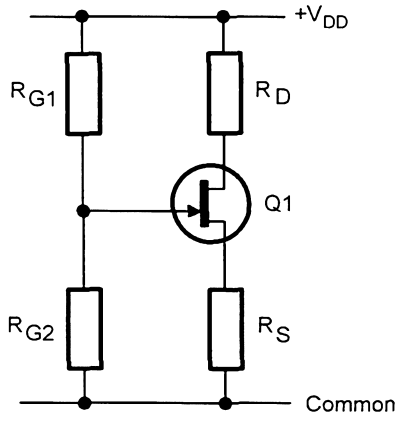
7. Identify typical biasing circuits used for N-channel and P-channel JFETs

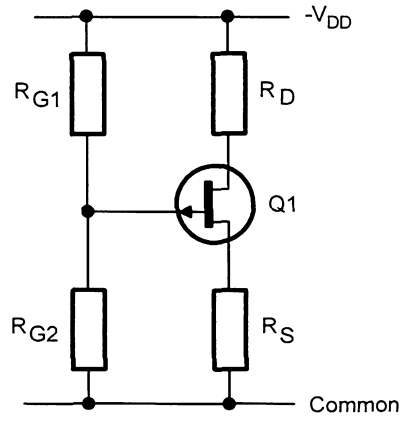
Examples of self bias:





Examples of voltage divider bias:





8. Explain the function of each component in the self bias and voltage divider bias JFET circuits

Self bias:

R_G clamps the gate to zero volts.

Q_1 converts variations in gate-source voltage to variations in drain-source current.

R_S sets the drain-source current (I_{DS}) and the source voltage (V_S).

R_D provides a path for the drain current to flow. It also sets up the quiescent DC drain voltage (V_D) and converts changes in drain-source current to changes in drain voltage.

Voltage divider bias:

R_{G1} ***and*** R_{G2} set the gate voltage.

Q1, R_S and R_D all perform the same functions as in the self bias circuit.

9. Calculate the voltages around self biased and voltage divider biased JFET circuits

Self bias (both N-channel & P-channel)

$V_G = 0V$

$V_S = V_G - V_{GS}$ (V_{GS} is given)

$I_{DS} = \frac{V_S}{R_S}$

$V_D = V_{DD} - (I_{DS} \times R_D)$

$V_{DG} = V_D - V_G$

$V_{DS} = V_D - V_S$

Voltage divider bias (both N-channel & P-channel)

$V_G = V_{DD} \times \frac{R_{G2}}{R_{G1}+R_{G2}}$

All other calculations are identical to those for the self bias circuit.

Section 7

Objectives and Summary

1. Identify the three JFET amplifier configurations

   To do this, look at the circuit's input and output connections (you don't even have to know which one is which!). The configuration is called a "Common _____ " where the missing word is the same as the pin not being used for the signal's input and output. So:

   a) Input to gate, output from drain so the circuit must be a Common Source
   b) Input to gate, output from source so the circuit must be a Common Drain
   c) Input to source, output from drain so the circuit must be a Common Gate

2. Identify the input and output terminals of each configuration

   Only two pins are used relative to common. Importantly...

   - Where the JFET's drain pin is used, it is only ever as an output
   - Where the JFET's gate pin is used, it is only ever as an input
   - Where the JFET's source pin is used, it can be an input (CG) or an output (CD)

3. Describe the effects on the quiescent voltages and currents around the JFET configurations when an input signal is connected

   Key
   ↑ means "goes up"
   ↓ means "goes down"

   Common source

   As Vin ↑, V_G ↑ so V_{GS} ↓. This causes I_{DS} ↑, which means V_{RD} ↑, and so V_D ↓
   As Vin ↓, V_G ↓ so V_{GS} ↑. This causes I_{DS} ↓, which means V_{RD} ↓, and so V_D ↑

   Common drain

   As Vin ↑, V_G ↑ so V_{GS} ↓. This causes I_{DS} ↑ and so V_{RS} ↑
   As Vin ↓, V_G ↓ so V_{GS} ↑. This causes I_{DS} ↓ and so V_{RS} ↓

4. State the signal input-output phase relationship for each configuration

   Common Source: The output is inverted compared to the input
   Common Drain: The output is in-phase with the input
   Common Gate: The output is in-phase with the input

5. Calculate (using approximation equations) the voltage gain, input resistance and output resistance for the common source amplifier configuration

   $Av_{(unloaded)} = Gm \times R_D$ or $Av_{(loaded)} = Gm \times (R_D // R_L)$

   $Rin = R_G$ (Self bias) or $Rin = R_{G1} // R_{G2}$ (Voltage divider bias)

   $Rout = R_D$

6. Calculate (using approximation equations) the voltage gain, input resistance and output resistance for the common drain amplifier configuration

   $Av_{(unloaded)} = \frac{Gm \times R_S}{1+(Gm \times R_S)}$

   $Rin = R_G$ (Self bias) or $Rin = R_{G1} // R_{G2}$ (Voltage divider bias)

   $Rout \approx \frac{1}{Gm}$

7. State the two factors that determine the maximum peak-to-peak output voltage of a JFET amplifier

   - The supply voltage
   - The quiescent DC voltage on the JFET's pin that is the output

   [The amount of loading affects this too but that's not an issue dealt with in this Unit.]

8. Calculate the maximum peak-to-peak output voltage of a JFET amplifier

If the voltage on the output lead is less than half of the supply voltage then the maximum peak-to-peak output voltage is found using the equation:

Common source: $Vout_{(max)} = V_D \times 2$

Common drain: $Vout_{(max)} = V_S \times 2$

If the voltage on the output lead is more than half of the supply voltage then the maximum peak-to-peak output voltage is found using the equation:

Common source: $Vout_{(max)} = (V_{DD} - V_D) \times 2$

Common drain: $Vout_{(max)} = (V_{DD} - V_D) \times 2$

Note: This is an oversimplification and assumes the circuit is unloaded or lightly loaded.

9. Interpret manufacturers' data on JFETs

When you look-up JFET data sheets, the main performance characteristics that you are likely to need to look for include:

- Package (or case)
- Pinout
- N-channel or P-channel
- $V_{GS(off)}$
- V_{DS} (maximum rating)
- V_{DG} (maximum rating)
- I_{DSS}
- Power rating
- Transconductance (*Gm*)

10. Measure the DC voltages around the circuit of various JFET amplifier circuits

    See the Skill Practice Exercise.

11. Measure the gain, phase relationship and maximum peak-to-peak output voltage of a common source and common drain JFET amplifier

    See the Skill Practice Exercise.

12. Measure the frequency response of JFET amplifiers

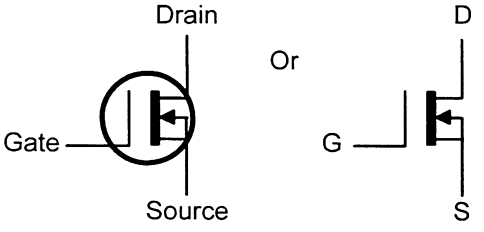
    See the Skill Practice Exercise.

Section 8

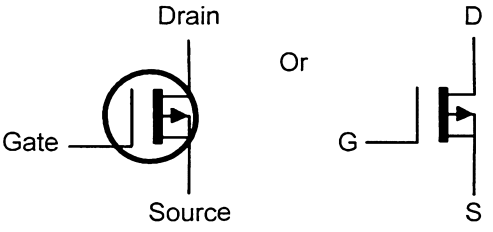
Objectives and Summary

1. Draw and identify the schematic symbols for depletion and enhancement mode MOSFETs

Depletion mode MOSFET

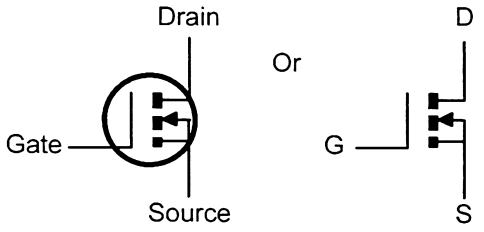


N-channel

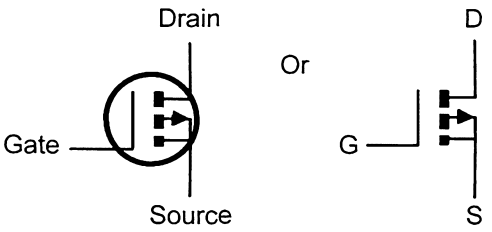


P-channel

Enhancement mode MOSFET



N-type



P-type

2. Describe the bias conditions needed for each junction of a MOSFET for it to operate in amplifier circuits

Depletion mode MOSFET (biased to operate entirely or mostly in the depletion mode)

N-channel: Drain must be the most positive of the three terminals, then the source, then the gate.

P-channel: Drain must be the most negative of the three terminals, then the source, then the gate.

Note: These conditions are the same as for the JFET.

Depletion mode MOSFET (biased to operate in both the depletion and enhancement modes)

N-channel: Drain must be the most positive of the three terminals. The source and the gate are the same voltage (and typically zero).

P-channel: Drain must be the most negative of the three terminals. The source and the gate are the same voltage (and typically zero).

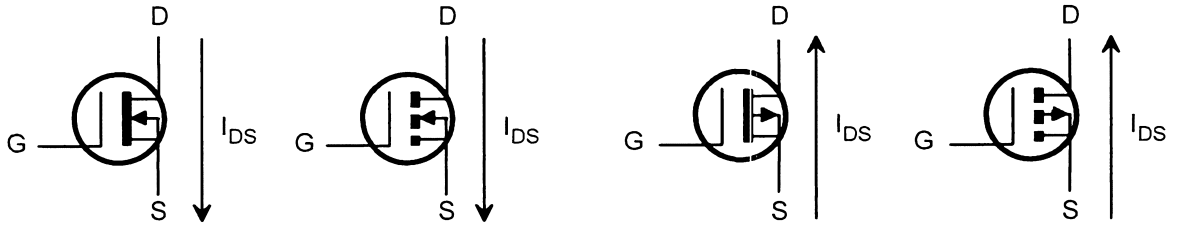
Enhancement mode MOSFET

N-type: Drain must be the most positive of the three terminals, then the gate then the source.

P-type: Drain must be the most negative of the three terminals, then the gate then the source.

Note: These conditions are the same as for the BJT (only the terminal names are different).

3. Show the direction of current flow and voltage polarity at each terminal of the MOSFET



N-channel/type **P-channel/type**

4. Explain the operating principles of MOSFETs

Depletion mode

The Depletion mode MOSFET is a voltage-controlled device. Drain-source current flows when:

- there is either a negative or a positive potential difference between the gate and the source ($\pm V_{GS}$) for both the N-channel and P-channel devices.

Moreover, the amount of drain current is a function of the size of gate-source voltage. That is:

- as V_{GS} gets smaller and goes negative, drain current goes down for the N-channel MOSFET.
- as $-V_{GS}$ gets smaller and goes positive, drain current goes down for the P-channel MOSFET.

Enhancement mode

The Enhancement mode MOSFET is a voltage-controlled device. Drain-source current flows when:

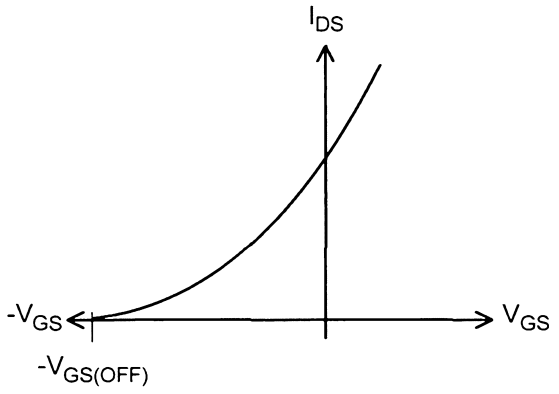
- there is a positive potential difference between the gate and the source ($+V_{GS}$) for the N-type MOSFET.
- there is a negative potential difference between the gate and the source ($-V_{GS}$) for the P-type MOSFET.

Moreover, the amount of drain current is a function of the size of gate-source voltage. That is:

- as V_{GS} becomes more positive, drain current goes up for the N-type MOSFET.
- as $-V_{GS}$ becomes more negative, drain current goes up for the P-type MOSFET.

5. Interpret graphs for MOSFET input-output transfer characteristics

Depletion mode N-channel MOSFET



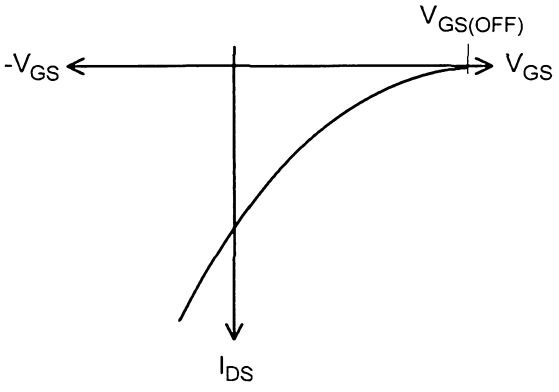
This graph tells us three things:

i) Maximum or "saturation" drain-source current (I_{DSS}) flows at some point when the gate is positive relative to the source.

ii) As the gate voltage becomes less positive relative to the source and then more negative, the drain-source current (I_{DS}) goes down.

iii) When the gate voltage is sufficiently negative relative to the source, the drain-source current (I_{DS}) is zero.

Depletion mode P-channel MOSFET



This graph tells us three things:

i) Maximum or "saturation" drain-source current (I_{DSS}) flows at some point when the gate is negative relative to the source.

ii) As the gate voltage becomes less negative relative to the source and then more positive, the drain-source current (I_{DS}) goes down.

iii) When the gate voltage is sufficiently positive relative to the source, the drain-source current (I_{DS}) is zero.

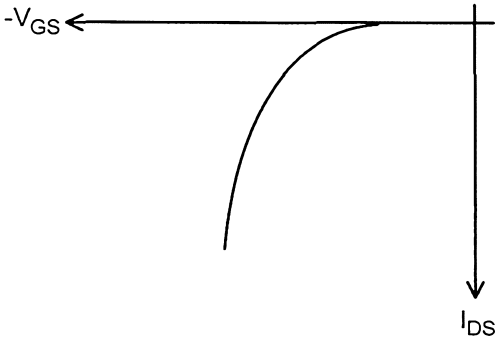
Enhancement mode N-type MOSFET

This graph tells us two things:

i) When the gate voltage is the same as the source voltage, the drain-source current (I_{DS}) is zero.

ii) The device only begins to conduct current when the gate voltage is made sufficiently positive relative to the source.

Enhancement mode P-type MOSFET



This graph tells us two things:

i) When the gate voltage is the same as the source voltage, the drain-source current (I_{DS}) is zero.

ii) The device only begins to conduct current when the gate voltage is made sufficiently negative relative to the source.

Note: These graphs are very similar to the graphs of the V_{BE}-I_C transfer characteristics of BJTs.

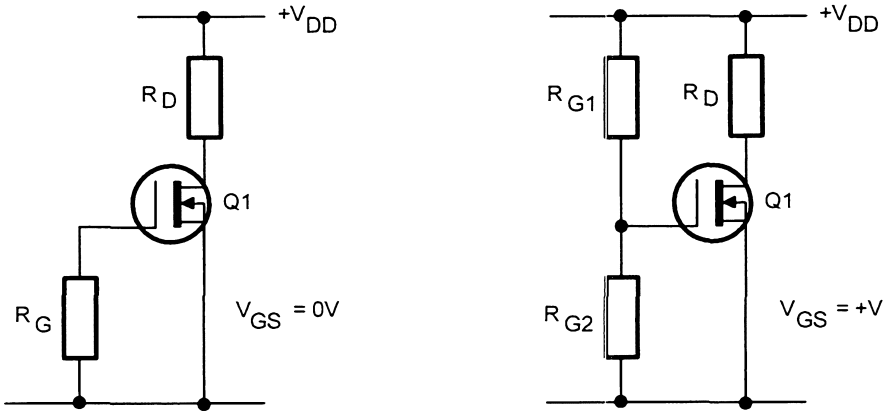
6. Identify the similarities and differences between MOSFET and JFET biasing circuits

Depletion mode MOSFETs (biased to operate entirely or mostly in the depletion mode)

- The self bias and voltage divider bias circuits for this device **and** this mode of operation are identical to the self-bias and voltage divider biased JFET circuits.

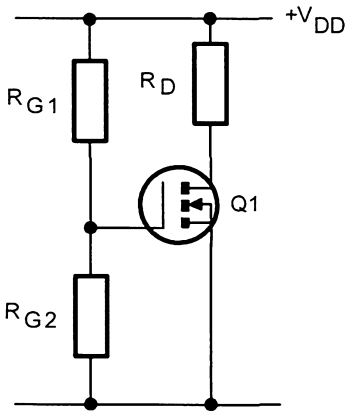
Depletion mode MOSFETs (biased to operate in both the depletion and enhancement modes)

- The biasing circuits for this device and mode of operation are a little different to the self-bias and voltage divider biased JFET circuits. Examples are shown below (using N-channel devices only). As you can see, a source resistor is not necessarily needed.



Enhancement mode MOSFETs

- Only voltage divider biasing is used for this device and this is shown using an N-type device. As you can see, a source resistor is not necessarily needed.



7. Calculate the voltages around MOSFET biasing circuits

Depletion mode MOSFETs (biased to operate entirely or mostly in the depletion mode)

Self bias (both N-channel & P-channel)

$V_G = 0V$

$V_S = V_G - V_{GS}$ (V_{GS} is given)

$I_{DS} = \frac{V_S}{R_S}$

$V_D = V_{DD} - (I_{DS} \times R_D)$

$V_{DG} = V_D - V_G$

$V_{DS} = V_D - V_S$

Voltage divider bias (both N-channel & P-channel)

$V_G = V_{DD} \times \frac{R_{G2}}{R_{G1}+R_{G2}}$

All other calculations are identical to those for the self bias circuit.

Note: These calculations are the same as for the equivalent JFET biasing circuits.

Depletion mode MOSFETs (biased to operate in both the depletion and enhancement modes)

$V_G = V_{DD} \times \frac{R_{G2}}{R_{G1}+R_{G2}}$

$V_S = 0V$

$I_{DS} = \frac{V_{RD}}{R_D}$

$V_D = V_{DD} - V_{RD}$ or $V_D = V_{DD} - (I_{DS} \times R_D)$ depending on the info provided.

$V_{DG} = V_D - V_G$

$V_{DS} = V_D - V_S$

Enhancement mode MOSFETs

All other calculations are identical to those for the Depletion mode MOSFETs (biased to operate in both the depletion and enhancement modes).

8. Identify the similarities and differences between MOSFET and JFET amplifier configurations

   All MOSFET configurations are the same as JFET configurations and are identified in the same way.

9. Calculate the voltage gain, input resistance and output resistance of common source and common drain MOSFET amplifiers

   Common Source

   $Av_{(unloaded)} = Gm \times R_D$ or $Av_{(loaded)} = Gm \times (R_D // R_L)$

   $Rin = R_G$ (Self bias) or $Rin = R_{G1} // R_{G2}$ (Voltage divider bias)

   $Rout = R_D$

   Note: This is the same as for the JFET Common Source amplifier.

   Common Drain

   $Av_{(unloaded)} = \frac{Gm \times R_S}{1+(Gm \times R_S)}$

   $Rin = R_G$ (Self bias) or $Rin = R_{G1} // R_{G2}$ (Voltage divider bias)

   $Rout \approx \frac{1}{Gm}$

   Note: This is the same as for the JFET Common Drain amplifier.

10. Measure the DC voltages around the circuit of various MOSFET amplifier circuits

    See the Skill Practice Exercise.

11. Measure the gain, phase relationship and maximum peak-to-peak output voltage of a common source and common drain MOSFET amplifier

    See the Skill Practice Exercise.

12. Measure the frequency response of MOSFET amplifiers

    See the Skill Practice Exercise.

Answers to review questions

Section 1

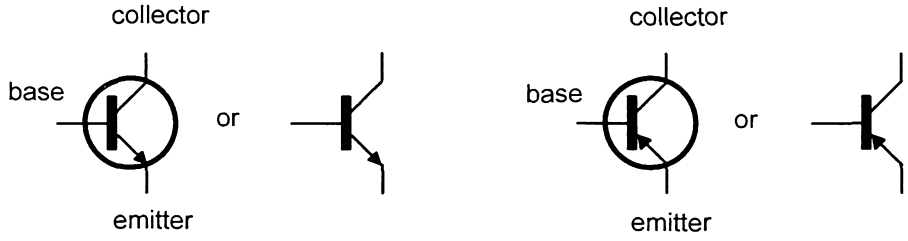
1. A transistor (BJT) is a current amplifying device. Changes in base current cause larger changes in collector current.

2. Silicon

3. Three (though some devices have only two but these use the transistor's case as the third pin)

4. NPN and PNP

5.



NPN BJT **PNP BJT**

6. See above.

7. Emitter

8. Direction of conventional current flow.

9. NPN

10. The term *bias* refers to the DC voltage and current requirements of the transistor.

11. Forward bias occurs when the polarity of the voltage across a PN junction allows it to conduct. Reverse bias occurs when the polarity of the voltage across a PN junction doesn't allow it to conduct.

12. The base-emitter junction must be forward biased.
The base-collector junction must be reverse biased.

13. The emitter current is the sum of the base and collector currents (that is, $I_E = I_B + I_C$).

14. The collector current is 200 times larger than the base current.

Section 1 (continued)

15. 250

16. Transposing $\beta = \frac{I_C}{I_B}$ to make I_B the subject gives . . .

$$I_B = \frac{I_C}{\beta}$$

$$I_B = \frac{2mA}{220}$$

$$I_B = 9.09\mu A$$

17. Transposing $\beta = \frac{I_C}{I_B}$ to make I_C the subject gives . . .

$$I_C = I_B \times \beta$$

$$I_C = 15\mu A \times 310$$

$$I_C = 4.65mA$$

18. $I_B = I_E - I_C$

$$I_B = 1.01mA - 1mA$$

$$I_B = 10\mu A$$

$$\beta = \frac{I_C}{I_B}$$

$$\beta = \frac{1mA}{10\mu A}$$

$$\beta = 100$$

19. 0.6V

20. Base current will go up.

21. Collector current will go down.

22. Cut-off is the condition of the transistor where there is no base current and therefore no collector current.

Section 1 (continued)

23. As we know, the greater the base current the greater the collector current. However, this is only up to a point. A transistor is said to be in saturation mode when further increases in base current no-longer cause increases in collector current.

Section 2

1. Base bias

2. Into the collector and out of the emitter

3. Into the base and out of the emitter

4. $V_B = 0.6V$

5. $I_B = \frac{V_{RB}}{R_B}$

   $I_B = \frac{12V - 0.6V}{1M2}$

   $I_B = 9.5\mu A$

6. $I_C = I_B \times \beta$

   $I_C = 9.5\mu A \times 200$

   $I_C = 1.9mA$

7. $V_C = Vcc - (I_C \times R_C)$

   $V_C = 12V - (1.9mA \times 3k3)$

   $V_C = 12V - 6.27V$

   $V_C = 5.73V$

8. The collector voltage (V_C) would decrease. This is because, if beta increases, the collector current (I_C) increases, which in turn increases the potential difference across the collector resistor (V_{RC}) leaving less voltage at the collector with respect to ground.

Section 2 (continued)

9. No, because the polarity of the voltages around the circuit would not forward bias the PNP transistor.

   [You could argue that the polarity of the voltages might be correct if the PNP BJT was put in the circuit with the emitter and collector pins swapped around. However, it still wouldn't work because the component values would not set up appropriate DC voltages around the circuit.]

10. Base bias.

11. Into the emitter and out of the collector

12. Into the emitter and out of the base

13. $V_B = -0.6V$

14. $I_B = \frac{V_{CC} - V_B}{R_B}$

    $I_B = \frac{-10V-(-0.6V)}{1M5}$

    $I_B = -6.27\mu A$ [Note: Don't be alarmed by the fact that the current is a negative value. This only indicates that the common line is sourcing the current instead of sinking it.]

15. $I_C = I_B \times \beta$

    $I_C = -6.27\mu A \times 150$

    $I_C = -940\mu A$

16. $V_C = V_{CC} - (I_C \times R_C)$

    $V_C = -10V - (-940\mu A \times 5k6)$

    $V_C = -4.74V$

17. Voltage divider biasing

Section 2 (continued)

18. $V_B = Vcc \times \frac{R2}{R1+R2}$

$V_B = 15V \times \frac{10k}{82k+10k}$

$V_B = 1.63V$

19. $V_E = V_B - 0.6V$

$V_E = 1.63V - 0.6V$

$V_E = 1.03V$

20. $I_C \approx I_E = \frac{V_{R4}}{R4}$

$I_C = \frac{1.03V}{470\Omega}$

$I_C = 2.19mA$

21. $V_C = Vcc - (I_C \times R3)$

$V_C = 15V - (2.19mA \times 3k3)$

$V_C = 7.77V$

22. $V_{CE} = V_C - V_E$

$V_{CE} = 7.77V - 1.03V$

$V_{CE} = 6.74V$

23. $V_{CB} = V_C - V_B$

$V_{CB} = 7.77V - 1.63V$

$V_{CB} = 6.14V$

24. R3 converts the collector current to a voltage.

25. R4 sets the collector current (by setting the emitter current).

Section 2 (continued)

26. R1 and R2 set the base voltage.

27. $V_B = Vcc \times \frac{R2}{R1+R2}$

$V_B = -18V \times \frac{12k}{12k+100k}$

$V_B = -1.92V$

28. $V_E = V_B + 0.6V$

$V_E = -1.92V + 0.6V$

$V_E = -1.32V$

29. $I_C \approx I_E = \frac{V_E}{R4}$

$I_C = \frac{-1.32V}{1k2}$

$I_C = -1.1mA$

30. $V_C = V_{CC} - (I_C \times R4)$

$V_C = -18V - (-1.1mA \times 8k2)$

$V_C = -8.98V$

31. $V_{CE} = V_C - V_E$

$V_{CE} = -8.98V - -1.32V$

$V_{CE} = -7.66V$

32. $V_{CB} = V_C - V_B$

$V_{CB} = -8.98V - -1.92V$

$V_{CB} = -7.06V$

Section 2 (continued)

33. 6k8Ω [If you're having trouble getting this answer, remember that the voltage you're given is the potential difference across the collector resistor and not the collector voltage.]

34.

V_B	V_E	V_C	Cause
0V	0V	12V	R1 open-circuit
1.7V	1.7V	12V	B-E short-circuit
2.2V	1.6V	12V	C open-circuit
4V	3.6V	4.4V	R2 high
2.2V	1.6V	4.4V	R3 high
2.2V	2.4V	2.4V	C-E short-circuit

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Section 3

1. Common emitter

2. Between 3 and 300

3. $Vout_{(max)} = (V_{CC} - V_c) \times 2$

   $Vout_{(max)} = (15V - 9.5V) \times 2$

   $Vout_{(max)} = 11V_{p-p}$

4. $Vin_{(max)} = \frac{Vout_{(max)}}{Av}$

   $Vin_{(max)} = \frac{11V}{120}$

   $Vin_{(max)} = 91.7mV_{p-p}$

5. Common base

6. Common collector

7. Common emitter

8. Emitter follower
   Buffer

9. Because the AC voltage on the emitter is the same as the input signal (that is, the emitter follows the base).

10. Common base

11. (a) Common collector
    (b) Common emitter
    (c) Common collector
    (d) Common base
    (e) Common emitter
    (f) Common collector

Section 3 (continued)

12. Common collector

13. Slightly less than 1

14. $Vout_{(max)} = V_E \times 2$

    $Vout_{(max)} = 8.4V \times 2$

    $Vout_{(max)} = 16.8V$

15. $Vin_{(max)}$ = slightly more than $16.8V$

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Section 4

1. $V_B = Vcc \times \frac{R_{B2}}{R_{B1}+R_{B2}}$

   $V_B = 10V \times \frac{15k}{82k+15k}$

   $V_B = 1.55V$

2. $V_E = V_B - 0.6V$

   $V_E = 1.55V - 0.6V$

   $V_E = 0.95V$

3. $I_C = I_E = \frac{V_E}{RE}$

   $I_C = \frac{0.95V}{680\Omega}$

   $I_C = 1.4mA$

   $V_C = Vcc - (I_C \times R_C)$

   $V_C = 10V - (1.4mA \times 3k3)$

   $V_C = 5.38V$

4. $r_e = \frac{26mV}{I_E}$

   $r_e = \frac{26mV}{1.4mA}$

   $r_e = 18.6\Omega$

5. $Av_{(unloaded)} = \frac{R_C}{r_e+R_E}$

   $Av_{(unloaded)} = \frac{3k3}{18.6\Omega+680\Omega}$

   $Av_{(unloaded)} = 4.72$

Section 4 (continued)

6. $Rin = R_{B1}//R_{B2}//\beta(r_e + R_E)$

   $Rin = 82k//15k//200 \times (18.6\Omega + 680\Omega)$

   $Rin = 82k//15k//139.7k$

   $Rin = 11.6k\Omega$

7. $Rout = R_C = 3k3\Omega$

8. Phase inverted

9. 9.24Vp-p

10. $Vin_{(max)} = \frac{Vout_{(max)}}{Av}$

    $Vin_{(max)} = \frac{9.24Vp-p}{4.72}$

    $Vin_{(max)} = 1.96V_{p-p}$

11. The voltage gain would go up because it is directly proportional to the collector resistor's value (proof: $Av = \frac{R_C}{R_E+r_e}$).

12. The voltage gain would go down because it is inversely proportional to the emitter resistor's value.

13. Very little because the design of this circuit produces a voltage gain that is largely independent of beta.

14. $V_B = 2.16V$

15. $V_E = 1.56V$

16. $I_C = 1mA$

    $V_C = 6.4V$

17. $r_e = 26\Omega$

Section 4 (continued)

18. $Av_{(loaded)} = \frac{R_C // R_L}{r_e}$

$Av_{(loaded)} = \frac{5k6 // 6k8}{26\Omega}$

$Av_{(loaded)} = 118$

19. $Rin = R_{B1} // R_{B2} // \beta r_e$

$Rin = 150k / 33k / (280 \times 26\Omega)$

$Rin = 5.74k\Omega$

20. $Rout = R_C = 5k6\Omega$

21. $Vin = \frac{Vout_{p-p}}{Av}$

$Vin = \frac{9V_{p-p}}{118}$

$Vin = 76.3mVp-p$

22. The output voltage would go up because the amplifier is no-longer loaded down.

23. The output voltage would go down because, with *C3* open, R_E would be providing negative feedback to the AC circuit as well as the DC circuit (and that makes the gain go down).

24. *Rin* goes up for the same reasons.

25. $I_E = 1.6mA$

$r_e = 16\Omega$

26. $Av_{(unloaded)} = \frac{R_C}{r_e}$

$Av_{(unloaded)} = \frac{3k9}{16\Omega}$

$Av_{(unloaded)} = 244$

Section 4 (continued)

27. $Rin = R_{B1}//R_{B2}//\beta \times r_e$

$Rin = 120k//22k//150 \times 16\Omega$

$Rin = 2126\Omega$

28. None. *C3* has no effect on DC.

29. $I_C = 5.4mA$

$r_e = 4.81\Omega$

30. $Av = \frac{R_E}{r_e + R_E}$

$Av = \frac{1k}{4.81\Omega + 1k}$

$Av = 0.995$

31. $Rin = R_{B1}//R_{B2}//\beta(r_e + R_E)$

$Rin = 22k//22k//\beta(4.81\Omega + 1k)$

$Rin = 10k6\Omega$

32. $Rout \approx r_e$

$Rout \approx 4.8\Omega$

33. In phase

34. There wouldn't be any noticeable change in the gain because the output resistance of the common collector configuration is so low.

35. 2.22V [If you're having trouble solving this question, follow this procedure: use the appropriate gain equation to calculate r_e then calculate I_E, V_E, and V_B.]

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Section 5

1. Signal too small
   Signal too big
   No output signal at all
   Signal clipped (when it shouldn't be for the size of the input signal)
   Signal distorted in some other way

2. It's inefficent
   You risk of damaging the printed circuit board
   You may introduce problems

3. You would first measure the circuit's power supply voltage (ie the *Vcc*).

4. If *Vcc* is not what it should be then all other voltages around the circuit will be not what they're supposed to be too. This can potentially mislead you into predicting the fault incorrectly.

5.

	V_B	V_E	V_C	Fault?
i)	6V	5.4V	6.7V	*R2* gone high
ii)	1.8V	1.2V	14V	*R4* gone high
iii)	0.9V	0.9V	18V	*Q1* base-emitter short-circuit
iv)	1.8V	1.2V	18V	*Q1* collector open-circuit
v)	1.8V	1.2V	0V	*R3* open-circuit
vi)	0V	0V	18V	*R1* open-circuit
vii)	1.8V	5V	5V	*Q1* collector-emitter short-circuit

6. The transistor type (Is it NPN or PNP?)
   Maximum power handling capabilities
   Maximum terminal voltages and currents
   What the transistor is made of (silicon or germanium?)
   Package (TO-92, TO-220, TO-3, etc?)
   Beta
   Lead configuration
   Maximum operating frequency

7. Connect the meter's black probe to the base and the other probe to the other two transistor leads (one at a time). The meter will read about 0.6V if the transistor is PNP and high if the transistor is NPN. If you think the transistor is NPN, reverse the meter probes and repeat the tests - the meter will read about 0.6V for both measurements.

Section 5 (continued)

8. (a) No. The BC549 is NPN and the BC559 is PNP.

(b) No. The MJ15003 is a power transistor and so has a lower beta, is physically much larger and has a totally different package.

(c) Yes. Though the packages are different so this might be a problem. (Note: although the maximum power characteristic of the two transistors is different, the BD140 can handle more power than the BD640 so it is ok to use. However, you probably wouldn't replace a BD140 with a BD640.)

(d) Yes. But be aware that the BC549 has lower noise characteristic which is why it might have been used instead of a BC548.

(e) Yes. Though the packages are different so this might be a problem

(f) No. The BF180 is a UHF amp and the BC337 is a small power amp.

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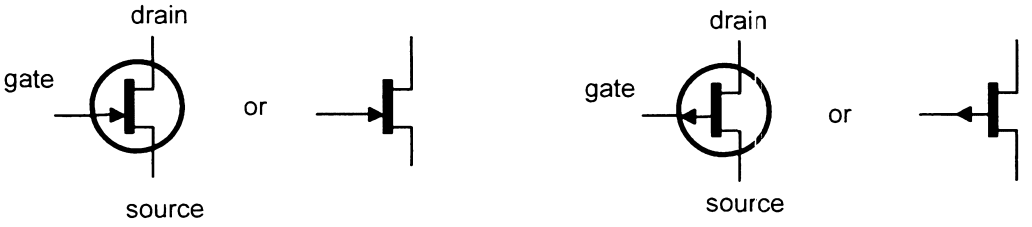
Section 6

1. Junction Field Effect Transistor

2. Lower noise, higher input resistance and they are not prone to thermal runaway.

3. Higher gain and higher operating frequency

4.



5. Because changes in drain-source current are caused by changes in gate voltage. (Note: this very different to BJTs where changes in collector-emitter current are caused by changes in base current.)

6. (a) The gate must be more negative than the source.
   (b) The drain must be more positive than the source.

7. Reverse biased in both cases.

8. (a) $V_{GS(off)}$ is the value of V_{GS} that causes I_{DS} to drop to 0A.
   (b) I_{DSS} is the maximum amount of I_{DS} (and occurs when $V_{GS} = 0V$).

9. Drain-source current (I_{DS}) goes down.

10. None. The gate-source junction is reversed biased. That's why the JFET is "voltage controlled".

11. Yes. The channel (between the drain and source) has a resistance of about 2kΩ each way.

12. V_G is "clamped" at 0V by R_G. V_S is at some positive voltage because I_{DS} develops a potential difference across R_S. And, since $V_{GS} = V_G - V_S$, V_{GS} must be a negative voltage and therefore the JFET is biased correctly.

Section 6 (continued)

13. $V_G = 0V$

14. $V_S = V_G - V_{GS}$

$V_S = 0V - (-1.5V)$

$V_S = 1.5V$

15. $I_{DS} = \frac{V_S}{R_S}$

$I_{DS} = \frac{1.5V}{1k\Omega}$

$I_{DS} = 1.5mA$

16. $V_D = V_{DD} - (I_D \times R_D)$

$V_D = 15V - (1.5mA \times 4k7)$

$V_D = 7.95V$

17. $V_{DS} = V_D - V_S$

$V_{DS} = 7.95V - 1.5V$

$V_{DS} = 6.45V$

18. (a) The JFET
(b) R_D
(c) R_G
(d) R_S

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Section 6 (continued)

19. $V_G = V_{DD} \times \frac{R_{G2}}{R_{G1}+R_{G2}}$

$V_G = 15V \times \frac{150k\Omega}{150k\Omega+1M\Omega}$

$V_G = 1.67V$

20. $V_S = V_G - V_{GS}$

$V_S = 1.67V - (-0.53V)$

$V_S = 2.2V$

21. $I_{DS} = 1.83mA$

22. $V_D = 7.86V$

23. $V_{DS} = 5.66V$

24. $V_G = 0V$

25. $V_S = 6.9V$

26. $I_{DS} = 2.1mA$

27. $V_D = V_{DD} = 15V$

28. $V_{DS} = 8.07V$

29. $V_{GS} = 0V$

30. $V_S = V_G - V_{GS}$

$V_S = 0V - (+2.25V)$

$V_S = -2.25V$

Section 6 (continued)

31. $I_{DS} = \frac{V_S}{R_S}$

$I_{DS} = \frac{-2.25V}{1k5}$

$I_{DS} = -1.5mA$ (Note: the negative sign indicates that the current flows from common up through the JFET to the negative supply rail.)

32. $V_D = V_{DD} - (I_D \times R_D)$

$V_D = -25V - (-1.5mA \times 10k)$

$V_D = -10V$

33. $V_{DS} = V_D - V_S$

$V_{DS} = -10V - (-2.25V)$

$V_{DS} = -7.75V$

34. There is no gate current.

35. Current flows from common into the JFET's source and out of its drain.

36.

V_G	V_S	V_D	Cause
0V	0V	14V	Drain or source open-circuit
0V	0V	0V	R2 open-circuit
3.6V	3.6V	6V	Gate-source short-circuit
0V	2.3V	6V	R2 high
0V	4V	4V	Drain-source short-circuit

Section 7

1. Common source

2. Phase inverted

3. $Av = Gm \times R_D$

   $Av = 3,000\mu S \times 4k7$

   $Av = 14.1$

4. $Rin = R_G = 1M\Omega$

5. $Rout = R_D = 4k7\Omega$

6. $Vout_{(max)} = (V_{DD} - V_D) \times 2$

   $Vout_{(max)} = (15V - 9.4V) \times 2$

   $Vout_{(max)} = 11.2V_{p-p}$

7. $Vin_{(max)} = \frac{Vout_{(max)}}{Av}$

   $Vin_{(max)} = \frac{11.2V}{14.1}$

   $Vin_{(max)} = 794mV_{p-p}$

8. The gain would go down.

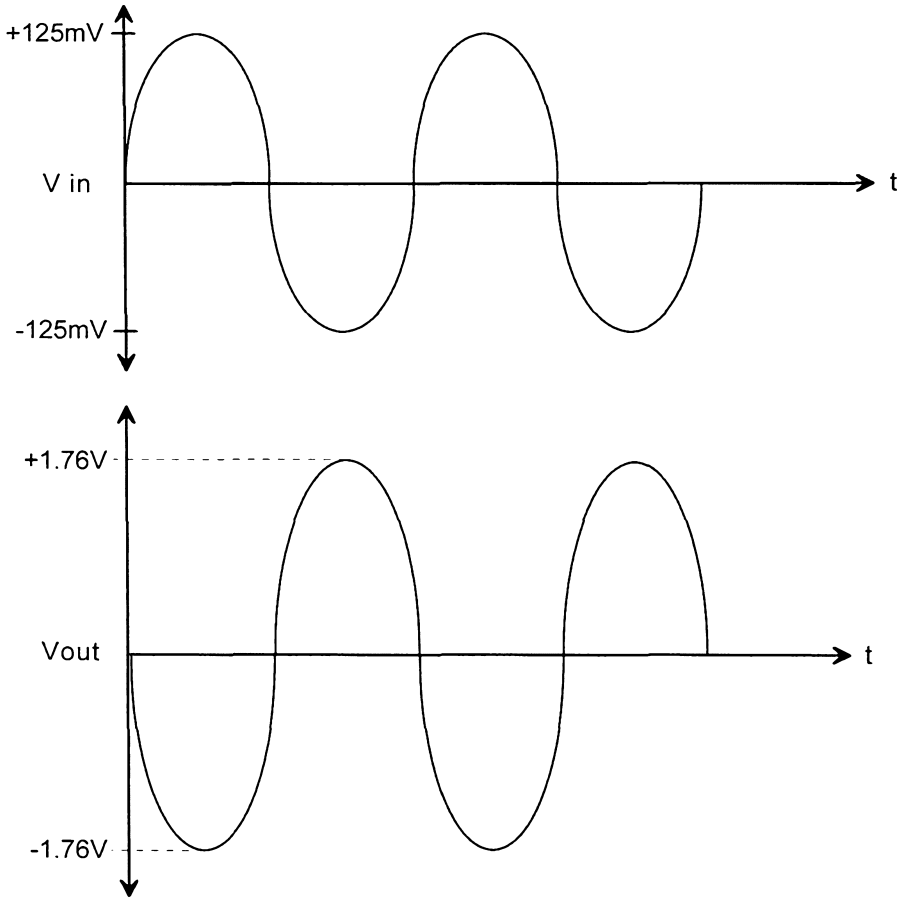
9. Provide a path for AC signals but block DC voltages to prevent the DC quiescent conditions from being upset.

Section 7 (continued)

10. $Vout = Vin \times Av$

$Vout = 125mV_{(pk)} \times 14.1$

$Vout = 1.76V_{(pk)}$



11. $Av_{(unloaded)} = 8.58$

12. $Av_{(loaded)} = Gm \times (R_D // R_L)$

$Av_{(loaded)} = 2,200\mu S \times (3k9\Omega // 2k2\Omega)$

$Av_{(loaded)} = 3.1$

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Section 7 (continued)

13. $Rin = 1M5\Omega$

14. $Rout = 3k9\Omega$

15. The loaded output voltage would increase also.

16. Common drain

17. In phase

18. $Av_{(unloaded)} = \frac{Gm \times R_S}{1+(Gm \times R_S)}$

$Av_{(unloaded)} = \frac{1800\mu S \times 3k3\Omega}{1+(1800\mu S \times 3k3\Omega)}$

$Av = \frac{5.94}{6.94}$

$Av = 0.856$

19. $Rin = 2M\Omega$

20. $Rout \approx \frac{1}{Gm}$

$Rout \approx \frac{1}{1800\mu S}$

$Rout \approx 556\Omega$

21. $Vout_{(\max)} = (V_{DD} - V_S) \times 2$

$Vout_{(\max)} = (15V - 8.5V) \times 2$

$Vout_{(\max)} = 13V_{p-p}$

22. $Vin_{(\max)} = \frac{Vout_{(\max)}}{Av}$

$Vin_{(\max)} = \frac{13V_{p-p}}{0.856}$

$Vin_{(\max)} = 15.2V_{p-p}$

Section 7 (continued)

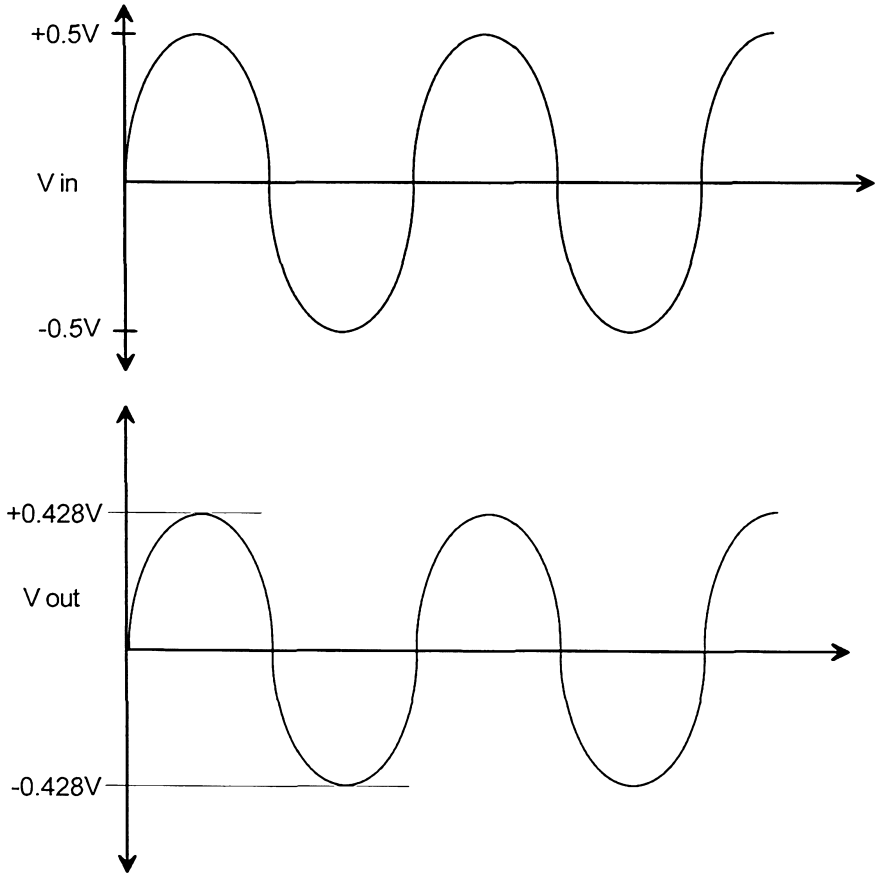
23. In most cases, the gain wouldn't change. The load resistance would have to be fairly low to cause the output voltage and gain to drop.

24. As a buffer circuit (also often referred to as *impedance matching*).

25. $Vout = Vin \times Av$

$Vout = 0.5V_{(pk)} \times 0.856$

$Vout = 0.428V_{(pk)}$



26. $Av_{(loaded)} = Gm \times (R_D // R_L)$

$Av_{(loaded)} = 4800\mu S \times (10k // 10k)$

$Av_{(loaded)} = 24$

Section 7 (continued)

27. $Rin = 1M\Omega$

28. $Rout = 10k\Omega$

Section 8

1. Advantage: Very low noise
   Disadvantage: Sensitive to electrostatic damage

2. Both depletion and enhancement modes

3. The gate voltage can be either positive or negative with respect to the source.

4. Enhancement mode only.

5. The gate voltage must be positive with respect to the source but not negative.

6. (a) The MOSFET
   (b) R_D
   (c) C2
   (d) C1
   (e) C_S
   (f) R_S

7. It can be either because it is a depletion-mode MOSFET which means it can operate in either the depletion or enhancement modes.

8. $V_G = 0V$

9. $V_S = 1.5V$

10. $V_D = 5.15V$

11. $V_{DS} = 3.65V$

12. $Vout_{(max)} = 7.7V_{p-p}$

13. Self bias

14. Common source

15. Phase inverted

Section 8 (continued)

16. $Av = 4.2$

17. $Rin = 2M\Omega$

18. $Rout = 1k\Omega$

19. $Vin_{(max)} = 1.83V_{p-p}$

20. Voltage gain would go down.

21. Isolate the amplifier stage from any DC in the source or load.

22. $Av = 1.7$

23. Self bias

24. Common drain

25. In phase

26. $Av = 0.82$

27. $Rin = 270k\Omega$

28. $Rout = 217\Omega$

29. Because the output resistance is relatively small.

30. The MOSFET is in the enhancement mode during the positive half cycle and depletion mode during the negative half cycle.

    To explain why, V_{GS} is 0V so the moment the input signal goes positive V_G becomes positive with respect to V_S and the MOSFET operates in enhancement mode. The moment the input signal goes negative V_G becomes negative with respect to V_S and the MOSFET operates in depletion mode.

31. $V_G = 3.2V$

32. $V_S = 5V$

33. $I_{DS} = 1.06mA$

    $V_D = 6.3V$

34. $Vout_{(max)} = 12.6V_{p-p}$

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Section 8 (continued)

35. Voltage divider biasing

36. Common source

37. Phase inverted

38. $Av = 20.5$

39. $Rin = R_{G1}//R_{G2}$

    $Rin = 1M//270k$

    $Rin = 213k\Omega$

40. $Rout = 8k2\Omega$

41. $Vin_{(max)} = 615mV_{p-p}$

42. Voltage divider biasing

43. Common drain

44. In phase

45. $Av = 0.85$

46. If R_{G1} became an open-circuit, V_G would drop to zero volts. This would make it impossible for the gate-source voltage to be positive so the MOSFET would turn off. (Note: there is still the possibility of an output signal if the +Vpk of the input signal was large enough but it would only be small positive going humps at the output.)

47. If the input signal was increased to 15Vp-p, the amplifier would be overdriven and clipping of the output signal would occur.